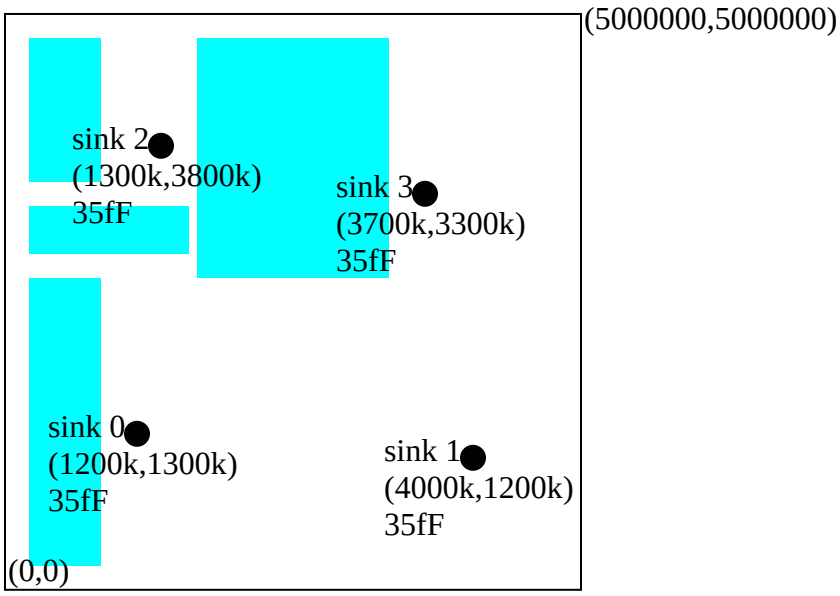
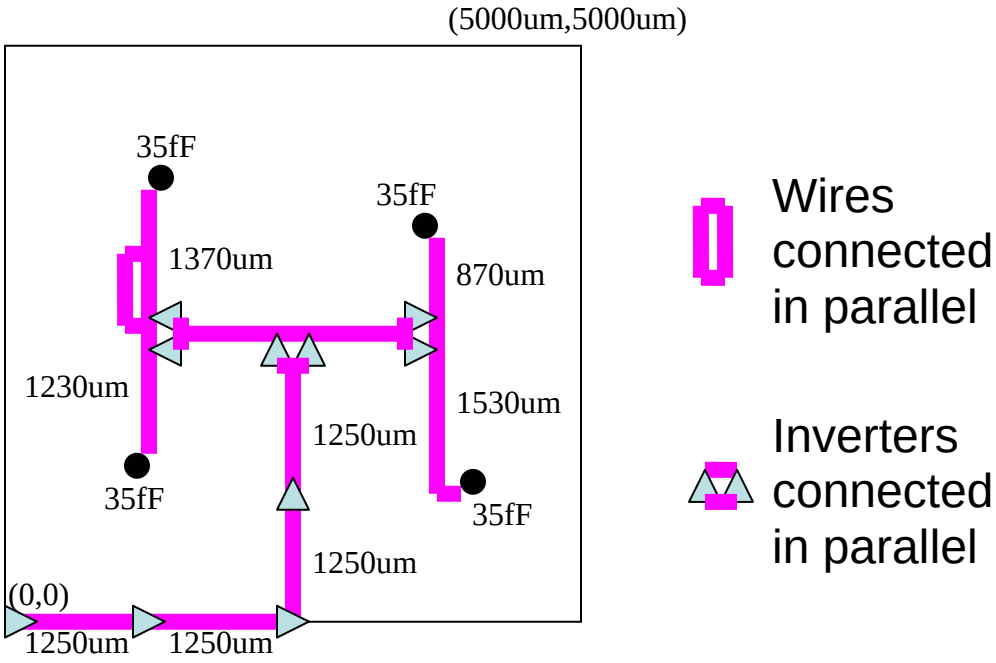
ISPD 2009 Clock Synthesis Contest

Pictures for explanation of the sample input/output files s1/s1s

In s1, there are four clock sinks, in the design area of 5mm x 5mm. It is depicted in the following figure. The coordinates are in nm. Blue boxes are placement blockages.



A sample (s1s) solution is shown in the following figure.



As you can see from the sample solution, the wire connecting the upper left sinks goes over the blockages but no buffer/inverter can be placed.

We make this contest simpler by removing the physical constraint of placement and routing. In other words, two inverters can be placed in at exact same location and two wires can be at the same routing track without any violation.