ACM International Symposium on Physical Design 2010
Clock Network Synthesis (CNS) Contest
Call for Participation

This is an announcement for the second clock network synthesis contest! During the past 5 years, ISPD has been hosting placement, routing and clock synthesis contests with relevant industrial benchmarks. In ISPD 2010, we continue this great tradition and organize an updated clock network synthesis contest. Clock distribution network synthesis is one of the most fundamental CAD problems, and with the ever increasing performance demands of today's VLSI chips, this problem is getting ever more difficult. In a typical industrial physical design flow for high-frequency microprocessors, a separate dedicated clock network synthesis process is applied to build high performance minimum skew clock network, making it an excellent candidate as our contest topic. As in previous contests, a new set of industrial clock network synthesis benchmarks will be released to further spur development in this area.

You are invited to participate!

Given a local clock skew target and a slew constraint, the quality of clock network solution will be measured by the total power dissipation. Skew and slew measurement will base on SPICE-level circuit simulation, considering both inverter and wire variations. In other words, a valid solution must meet the given slew constraint and local clock skew target. A valid solution must also be obstacle-aware, which means that it must be able to deal with blockages where clock inverters cannot be placed, but clock wires can route over blockages (since the clock typically uses a dedicated metal layer in any case). Compared to last year's CNS contest, we would like to make sure this contest aligns tighter with the state-of-the-art high-frequency microprocessor clock designs. Some of the other highlights are:

- Delay variation on wires will be formulated.
- All benchmarks will have more than 1000 clock sinks, which roughly approximates the clock pins on the hierarchical blocks seen by the chip level clock designs.
- Only local clock skew constraints will be enforced because early mode timing violations are usually limited in local regions.
- Simplified Monte Carlo simulation will be used to evaluate valid clock solutions.

Please make note of the following:

- The next ISPD will be held on March 14 - March 17, 2010 in San Francisco, California. The clock network synthesis contest will be held just prior to the symposium and the results will be announced during ISPD 2010.
- Cliff Sze from IBM Research will be the contest chair. Any question about the contest should be directed to **csze@us.ibm.com**, with **subject "ISPD2010-CNS"**.
- All contest details, file formats and materials will be posted at: http://www.ispd.cc/contests
- To enter the contest, you must register by **November 30, 2009** by sending an email to the contest chair. Include the name of the tool, the names of the developers and the affiliation.
- On **December 1, 2009**, we will post a few sample benchmarks, the exact format of the input and output files, the buffer and wire library and their parasitic models for circuit simulation. Also, a script to translate your clock network synthesis output file into SPICE simulation input file will be provided.
- By **January 10, 2010**, each team must submit an "alpha-version" executable and a script to test it on our platforms. This is very important to make sure that our simulation results match yours.
- By **January 31, 2010**, a final-version executable, a script and a one-page description of your algorithm must be submitted to the contest chair.