

ACM International Symposium on Physical Design 2012

Discrete Gate Sizing Contest

Call for Participation

Start Date: **October 10th, 2011**

Registration Deadline: **December 12th, 2011**

Use of Synopsys's PrimeTime* tool is encouraged. Contestants are encouraged to apply for a free license early. See below for details.

This is an announcement for the 1st ISPD contest on multi-core gate sizing and threshold voltage (Vt) assignment. During the past few years, ISPD has been hosting placement, routing and clock network synthesis contests with challenging industrial benchmarks. These contests have significantly advanced the quality of algorithms for physical design. In ISPD 2012, we continue this great tradition and host a new contest for simultaneous gate sizing and Vt assignment to optimize performance and power.

Gate sizing and Vt assignment is one of the most fundamental CAD problems in physical synthesis. Due to the increasing design sizes and more stringent timing requirements, gate sizing and Vt assignment has become an ever more difficult task for advanced designs.

- Very large designs require sizing algorithms to be scalable enough.
- The design variables (gate sizes or Vts) are based on standard cells and make the problem discrete.
- Realistic timing and physical constraints may lead to non-convex problems.

In a typical industrial physical synthesis flow, it usually takes multiple iterations to globally or locally optimize the gate sizes and Vt, making it an excellent candidate as a new contest topic. For those interested or experienced in this topic,

YOU ARE INVITED TO PARTICIPATE!

In the spirit of the past ISPD contests, a set of challenging realistic benchmarks with reduced complexity will be released to test the quality of the submitted algorithms. The benchmarks will come with standard cell libraries containing discrete gate size and Vt choices. The timing model will be realistic. Nevertheless, those with little timing background are encouraged to participate, because contestants will be allowed to use an industrial timing engine (Synopsys PrimeTime) as a black box during their optimization (see details below). The contestants can use any technique to come up with their solution. The quality of the solution will primarily be measured by the following metrics:

- Meeting max delay timing constraints
- Meeting slew requirements
- Minimizing design leakage
- Overall run time of the algorithm. *Multi-core implementations are encouraged!*

Detailed metric descriptions and contest rules will be released later on the contest website (http://www.ispd.cc/contests/12/ispd2012_contest.html). Some of the other highlights are:

- The delay model will be look-up table.
- Slew is considered as an important metric.
- Cell delay is not a convex function of cell size.
- Interconnect is modeled as a lumped capacitance (zero-R) and will be included in the timing evaluation.
- The contestants will be allowed to use Synopsys PrimeTime* (an industrial timing engine) as a black box during their optimization. The final evaluation will be done using this same timing engine. If you plan on using Synopsys PrimeTime and do not have it available at your university, please contact your university staff and Synopsys immediately to obtain a free license for academic use. Contest organizers may be able to help in this process in limited capability.
- Scripts will be provided to contestants to call Synopsys PrimeTime as a black box for timing evaluation.

Please make note of the following:

- The next ISPD will be held **March 25-28, 2012**, in San Francisco Bay Area, California, USA. The discrete gate sizing contest will be held just prior to the symposium. The contest will officially start on **October 10th, 2011**. To participate, contestants must register by **December 12th, 2011**. Please see the website for details
- The sample benchmarks and relevant scripts will be provided on **October 10th, 2011**, to test your tools.
- The contestants will be required to make their final submissions by **middle February, 2012**. Each team must ALSO MAKE an alpha binary submission for compatibility test two weeks before the final deadline.
- For registration or any other inquiries, please send emails to Cheng Zhuo (cheng.zhuo@intel.com).
- Please add "ISPD2012" to your subject line for any emails.
- For registration, please include the following information
 - Affiliation of the team/contestant
 - Names of team members
 - Synopsys PrimeTime license availability
 - One email address as the corresponding address of the team
- Further details like contest timelines, file formats, benchmark details, etc. will be announced later on the contest website.

Contest organizers:

Chirayu Amin	Intel Corporation
Andrey Ayupov	Intel Corporation
Steven Burns	Intel Corporation
Mustafa Ozdal (Contest chair)	Intel Corporation
Gustavo Wilke	Intel Corporation
Cheng Zhuo	Intel Corporation

* Other names and brands may be claimed as the property of others. *Note that there are many excellent static timing tools, and there is good correlation between them. In order to ensure uniformity in comparison, we have opted to use Synopsys PrimeTime as the reference to evaluate submissions; most research groups have easy access to the tool.*