ACM International Symposium on Physical Design 2013

Discrete Gate Sizing Contest

Call for Participation

Start Date: ***October 8th, 2012***
Registration Deadline: ***December 14th, 2012***

Use of Synopsys's PrimeTime* tool is encouraged. Contestants are encouraged to apply for a free license early. See below for details.

This is an announcement for the *2nd* ISPD contest on multi-core gate sizing and threshold voltage (Vt) assignment. During the past few years, ISPD has been hosting placement, routing, and clock network synthesis with challenging industrial benchmarks. These contests have significantly advanced the quality of algorithms for physical design. In the last year's ISPD contest, we hosted the 1st discrete gate sizing contest, in which we exposed some of the physical synthesis challenges to the academic community, while keeping the problem complexity still manageable. 18 teams completed the contest and presented very exciting results. In ISPD 2013, we continue this great tradition and host an updated contest for simultaneous gate sizing and Vt assignment to optimize performance and power.

Gate sizing and Vt assignment is one of the most fundamental CAD problems in physical synthesis. Due to the increasing design sizes and more stringent timing requirements, gate sizing and Vt assignment has become an ever more difficult task for advanced designs. In a typical industrial physical synthesis flow, it usually takes multiple iterations to globally or locally optimize the gate sizes and Vt, making it an excellent candidate as a contest topic. For those interested or experienced in this topic,

YOU ARE INVITED TO PARTICIPATE!

As in previous contests, a new set of realistic benchmarks will be released to further spur development in this area. The benchmarks will come with new standard cell libraries containing discrete gate size and Vt choices. The timing model will be more realistic by accounting for interconnect resistance and capacitance parasitics. Nevertheless, those with little timing background are encouraged to participate, because contestants will be allowed to use an industrial timing engine (Synopsys PrimeTime) as a black box during their optimization (see details below). The contestants can use any technique to come up with their solution. The quality of the solution will primarily be measured by the following metrics:

- Meeting max delay timing constraints
- Meeting slew requirements
- Minimizing design leakage
- Overall run time of the algorithm. *Multi-core implementations are encouraged!*

Detailed metric descriptions and contest rules will be released later on the contest website (http://www.ispd.cc/contests/13/ispd2013_contest.html). The differences from last year's contest are:

- A new set of more realistic and challenging benchmarks will be released.

- The interconnect model for each net will be a realistic RC tree instead of one lumped capacitance number.
- The contestants can choose to write their own Synopsys PrimeTime® (an industrial timing engine) script to collect timing information. The final evaluation will be done using this same timing engine. If you plan on using Synopsys PrimeTime® and do not have it available at your university, please contact your university staff and Synopsys immediately to obtain a free license for academic use. Contest organizers may be able to help in this process in limited capability.

Some of the other highlights are:

- The delay model will be look-up table.
- Slew is considered as an important metric.
- Cell delay is not a convex function of cell size.

Please make note of the following:

- The next ISPD will be held ***March 24-27, 2013,*** in Lake Tahoe vicinity, California, USA. The discrete gate sizing contest will be held just prior to the symposium. The contest will officially start on ***October 8th, 2012***. To participate, contestants must register by ***December 14th, 2012***. Please see the website for details
- The sample benchmarks and relevant scripts will *be provided by* ***middle November, 2012,*** to test your tools. The final benchmark release will be by ***middle January, 2013***.
- The contestants will be required to make their final submissions by ***middle February, 2013***. Each team must ALSO MAKE an alpha binary submission for compatibility test approximately two weeks before the final deadline.
- For registration or any other inquiries, please send emails to the following address (ispd2013contest@gmail.com).
- Please add "ISPD2013" to your subject line for any emails.
- For registration, please include the following information
  - Affiliation of the team/contestant
  - Names of team members
  - Synopsys PrimeTime® license availability
  - One email address as the corresponding address of the team
- Further details like contest timelines, file formats, benchmark details, etc. will be announced later on the contest website.

Contest organizers:

Chirayu Amin	Intel Corporation
Andrey Ayupov	Intel Corporation
Steven Burns	Intel Corporation
Mustafa Ozdal	Intel Corporation
Gustavo Wilke	Intel Corporation
Cheng Zhuo	Intel Corporation

* Other names and brands may be claimed as the property of others. *Note that there are many excellent static timing tools, and there is good correlation between them. In order to ensure uniformity in comparison, we have opted to use Synopsys PrimeTime® as the reference to evaluate submissions; most research groups have easy access to the tool.*