ACM International Symposium on Physical Design 2016

ROUTABILITY-DRIVEN FPGA PLACEMENT CONTEST

Call for Participation

Registration start date: November 9, 2015

Registration deadline: December 31, 2015

Web site: http://www.ispd.cc/contests/16/ispd2016_contest.html

E-mail: ispd2016contest@gmail.com

Since 2005, the ACM International Symposium on Physical Design (ISPD) has held a yearly EDA competition. Teamsô contributions have significantly advanced gate sizing, placement, global routing, and clock tree synthesis in ASIC design world.

We now announce the 2016 ISPD contest in a completely new area: FPGA design world. FPGAs are becoming more and more popular in all electronic applications, and FPGA design size kept growing over the last several decades. There are more and more challenging FPGA physical design problems that need to be addressed. The goal of the contest is to encourage academic research on FPGA design tools.

BENCHMARK DESCRIPTION:

The organizers will provide a benchmark suite using enhanced bookshelf format. Each design in the benchmark suite will have the following files:

1) design.aux: Auxilary file listing the files as the input of the placer;
2) design.nodes: (enhanced) Specifies instance/object attributes (name, master cell and dimensions etc.);
3) design.nets: Specifies the set of nets in the design;
4) design.pl: Specifies the location of the instances/objects including I/O and fixed instance locations;
5) design.scl: (enhanced) Extended from the original bookshelf format to represent FPGA placeable area and architecture specific placement information
6) design.wts: Currently unused as all instances/objects and nets have the same weight;
7) design.shapes: (new) Specifies the shapes/groups of the instances/objects that are placed together

Note that the FPGA architecture used in the contest will be based on Xilinx Ultrascale device. Xilinx reserves the right to modify the contents of the benchmark designs and format.

PLACEMENT EVALUTION:

The placement produced by participating placers will be evaluated by Vivado Router from Xilinx Inc. Xilinx will provide Vivado software and an integration flow that can read bookshelf format placement, check placement legality and perform routing.

The resulting placement will be evaluated by the following criteria:

1) Legality of the placement
2) Routability of the placement (routable or not within a time-out limit, 12 hours)
3) Routed total wirelength
4) Placement runtime

The details of the metrics and scoring system will be released after the contest registration.

RELEVANT CONTEST DATES:

Please make note of the following dates:

- To test your tools, a sample benchmark will be provided by November 1, 2015.
- More testing benchmarks will be released by December 18, 2015.
- To officially participate, contestants must register by December 31, 2015. Please see the registration section below or http://www.ispd.cc/contests/16/ispd2016_contest.html.
- Each team must submit an alpha binary submission by February 15, 2016 for testing purposes, else will be disqualified from the contest.
- Teams are required to submit their final executable binaries by midnight March 7, 2016.
- The organizers will run each teamôs placer in March 8-31, 2016.
- The contest results will be announced at the 2016 ISPD symposium (April 4-7, 2016) in California.

CONTEST REGISTRATION:

- For registration and contest related inquiries, please email: ispd2016contest@gmail.com.
- Please add "ISPD2016" to the subject line of any email.
- To register your team, please provide the following information:

1. Affiliation of the team/contestant(s)
2. Names of team members
3. One correspondence e-mail address for the team
4. Name of the placer

PRIZES:

There will be monetary prizes awarded to the top three teams. More details on this will be announced on the web site.

CONTEST ORGANIZERS:

Stephen Xiaojian Yang (Contest Chair)	Xilinx Inc.
Rajat Aggarwal	Xilinx Inc.
Aman Gayasen	Xilinx Inc.
Chandra Mulpuri	Xilinx Inc.
Ramine Roane	Xilinx Inc.

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