ACM International Symposium on Physical Design 2017

CLOCK-AWARE FPGA PLACEMENT CONTEST

Call for Participation

Registration start date: December 1, 2016

Registration deadline: January 31, 2017

Web site: http://www.ispd.cc/contests/17

E-mail: ispd2017contest@gmail.com

Since 2005, the ACM International Symposium on Physical Design (ISPD) has held a yearly EDA competition. Teamsô contributions have significantly advanced gate sizing, placement, global routing, and clock tree synthesis in ASIC and FPGA CAD area.

We now announce the 2017 ISPD contest as an extension over 2016 ISPD FPGA placement contest. This yearôs contest is still in FPGA placement area, with an emphasis on clock legalization and clock aware placement optimization. As FPGA designs become larger and more complex, the clocking structure in the designs need the tool to be able to optimize the placement while keeping legal clock solutions that match the device clocking architecture. The complexity of the problem provides good opportunity for participants to design and implement advanced algorithms.

BENCHMARK DESCRIPTION:

The organizers will provide a benchmark suite using enhanced bookshelf format. Each design in the benchmark suite will have the following files:

1) design.aux: Auxilary file listing the files as the input of the placer;
2) design.nodes: (enhanced) Specifies instance/object attributes (name, master cell and dimensions etc.);
3) design.nets: Specifies the set of nets in the design;
4) design.pl: Specifies the location of the instances/objects including I/O and fixed instance locations;
5) design.scl: (enhanced) Extended from the original bookshelf format to represent FPGA architecture, placeable area and clock architecture information;
6) design.wts: Currently unused as all instances/objects and nets have the same weight;

PLACEMENT EVALUTION:

The placement produced by participating placers will be evaluated by Vivado Place/Route tool from Xilinx Inc. Xilinx will provide Vivado software and an integration flow that can read bookshelf format placement, check clock placement legality and perform routing.

The detailed clocking legalization rule will be released on contest website.

The resulting placement will be evaluated by the following criteria:

1) Legality of the placement, including clock legalization and slice legalization
2) Routability of the placement (routable or not within a time-out limit, 12 hours)
3) Routed total wirelength
4) Total placement and routing runtime

The details of the metrics and scoring system will be released on contest website.

RELEVANT CONTEST DATES:

Please make note of the following dates:

- Placement benchmarks of ISPD 2016 contest will be available by November 30, 2016
- A new sample benchmark with clocking information will be provided by December 15, 2016
- More testing benchmarks will be released by January 10, 2017
- To officially participate, contestants must register by January 15, 2017. Please see the registration section below or http://www.ispd.cc/contests/17.
- Each team must submit an alpha binary submission by February 15, 2017 for testing purposes, else will be disqualified from the contest.
- All teams are required to submit their final executables by March 9, 2017.
- The organizers will run each teamôs placer in March 10-15, 2017.
- The contest winners will be announced at the 2017 ISPD symposium (March 19-22, 2017, Portland, OR, USA)

CONTEST REGISTRATION:

- For registration and contest related inquiries, please email: ispd2017contest@gmail.com.
- To register your team, please provide the following information:

1. Affiliation of the team/contestant(s)
2. Name of the placer
3. The correspondent author name and e-mail address
4. Names of all team members (can be changed later)

PRIZES:

There will be monetary prizes awarded to the top three teams. More details on this will be announced on contest web site.

CONTEST ORGANIZERS:

Stephen Yang (Contest Chair)	Xilinx Inc.
Rajat Aggarwal	Xilinx Inc.
Chandra Mulpuri	Xilinx Inc.
Srinivasan Dasasathyan	Xilinx Inc.
Sabya Das	Xilinx Inc.