Introduction of ISPD18 Contest Problem

Detailed routing can be divided into two steps. First, an initial detailed routing step is used to generate a detailed routing solution while handling the major design rules. Then a detailed routing refinement is performed to fix the remaining design rule violations. This proposed contest focuses on the initial detailed routing step. The quality of the initial detailed routing solution can be evaluated by the following aspects.

(1) Connectivity constraints
(2) LEF routing rules
(3) Routing preference metrics

According to these constraints/rules/metrics, we will come out a score for a given detailed routing solution, and the ranking of each participated team for the contest will be based on the scores. The details of these constraints/rules/metrics will be introduced in the following sections.

Connectivity Constraints

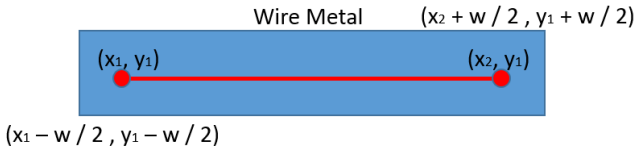
The connectivity constraint have to be satisfied in order to guarantee the valid signal and the routing wires that are able to be implemented. Therefore, the connectivity constraints have the highest priority to be obeyed.

1. OPEN

The pins of each net defined in *.input.def file need to be fully connected. If any pin in a net is disconnected, the net will be considered as an open net and huge score penalty will be applied.

2. SHORT

A wire metal is defined by the center line of a routing wire with a half wire width extension. Figure 1 shows a wire metal formed by a horizontal routing wire from (x1, y1) to (x2, y1) on the layer where wire width is *w*, which is specified by the WIDTH statement on each routing layer in LEF. On the other hand, a via metal is defined by the coordinate of a via with the metal extension defined in *.input.lef file. Figure 1 shows an example of via metal. Note that, ***in this contest, each layer has only one wire width***. Namely, non-default rule is not considered in this contest for simplicity. However, ***each layer may have one or multiple vias for choose to use.*** A short violation will happen when either a via metal or wire metal overlaps with another via metal, wire metal, blockages, or pin shapes. The intersection part between two objects are the short area.




```
VIA VIA45_2ST_S DEFAULT
    LAYER Metal4 ;
        RECT -0.035000 -0.325000 0.035000 0.065000 ;
    LAYER Via4 ;
        RECT -0.035000 -0.175000 0.035000 -0.105000 ;
    LAYER Metal5 ;
        RECT -0.065000 -0.175000 0.065000 0.035000 ;
END VIA45_2ST_S
```

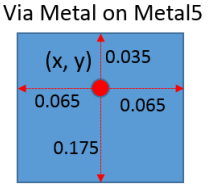


Figure 1

LEF Routing Rules

A detailed router need to consider many routing results defined in LEF files in order to meet the manufacturing requirements from foundries. Different technology nodes, different foundries, and different designs may have different routing rules. Because this contest focuses on the initial detailed routing step, so we only consider the most common and major routing rules. This section will briefly introduce these rules and how their syntax represent in LEF files. If you want to get more details about these routing rules, you can check the following document.
http://ispd.cc/contests/18/lefdefref.pdf

1. SPACINGTABLE

```
LAYER M1
TYPE ROUTING ;
SPACING 0.060000 ;
SPACINGTABLE
   PARALLELRUNLENGTH 0.000000
     WIDTH  0.000000  0.060000
     WIDTH  0.100000  0.100000
     WIDTH  0.750000  0.250000
     WIDTH  1.500000  0.450000 ;" ;
END M1
```

Specifies the spacing tables to use for wiring on the layer. The syntax for describing spacing tables is defined as follows:

```
SPACINGTABLE
  PARALLELRUNLENGTH {length} ...
    {WIDTH width {spacing} ...}... ;
```

Specifies the maximum parallel run length between two objects, in microns. If the maximum width of the two objects is greater than *width*, and the parallel run length is greater than *length*, then the spacing between the objects must be greater than or equal to *spacing*. The first spacing value is the minimum spacing for a given width, even if the PRL value is not met.

You must specify *length*, *width*, and *spacing* values in increasing order.
Type: Float, specified in microns (for all values)

When the parallel run length is greater than the first *length* in the table, then the spacing value in the respective row will be used (See Figure 2(a)). If the parallel run length is less than or equal to the first *length* in the table, then the default minimum spacing value defined by SPACING syntax will be used.

In general, the spacing table will contain multiple *length*s to represent different *spacing* values based on the parallel run length projections between the two objects. ***For the simplicity of the contest, we will reduce the number of lengths into one, thus the spacing value remain the same regardless of the parallel run length projection as long as it is greater than zero.***

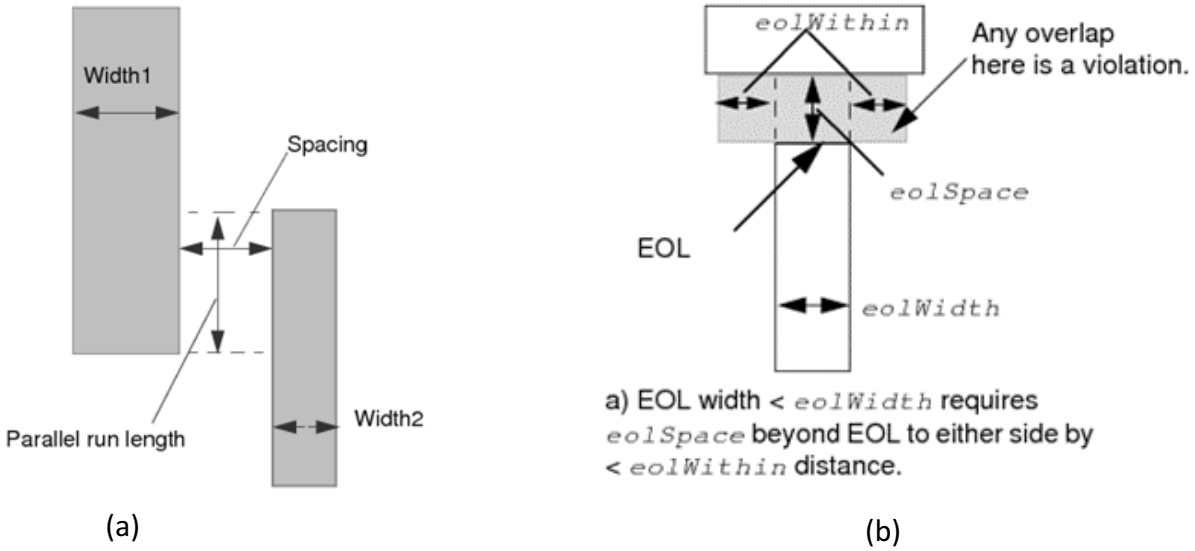


Figure 2

2. ENDOFLINE

LAYER M1
TYPE ROUTING ;
SPACING 0.090000 ENDOFLINE 0.090000 WITHIN 0.025000 ;
END M1

The syntax for describing EOL spacing rules is defined as follows:
SPACING *eolSpace* ENDOFLINE *eolWidth* WITHIN *eolWithin* ;

Indicates that an edge that is shorter than *eolWidth*, noted as end-of-line (EOL from now on) edge requires spacing greater than or equal to *eolSpace* beyond the EOL anywhere within (that is, less than) *eolWithin* distance (see Figure 2(b)).
Typically, *eolSpace* is slightly larger than the minimum allowed spacing on the layer. The *eolWithin* value must be less than the minimum allowed spacing.

3. CUT SPACING

LAYER V1
TYPE CUT ;
SPACING 0.070000 ;
END V1

Specifies the minimum spacing allowed between via cuts on the same net or different nets.

4. MIN AREA

LAYER Metal1
TYPE ROUTING ;
WIDTH 0.06 ;
AREA 0.02 ;

Specifies the minimum metal area required for polygons on the layer. All polygons must have an area that is greater than or equal to *minArea*. *Type:* Float, specified in microns squared

When a routed metal segment is small such that the whole polygon area will not satisfy the min area rule, a patch metal can be added to increase the area for the polygon. See Figure 3(a) to 3(c) for possible patch solution added to the existing metal routing to satisfy min area rule. However, the location and the size of the patch metal must be decided carefully so it will not cause any spacing or short violation. In addition, the overlapping region between patch and the existing metal routing must be greater or equal to the minimum *width* of the current routing layer (see Figure 3(d)).

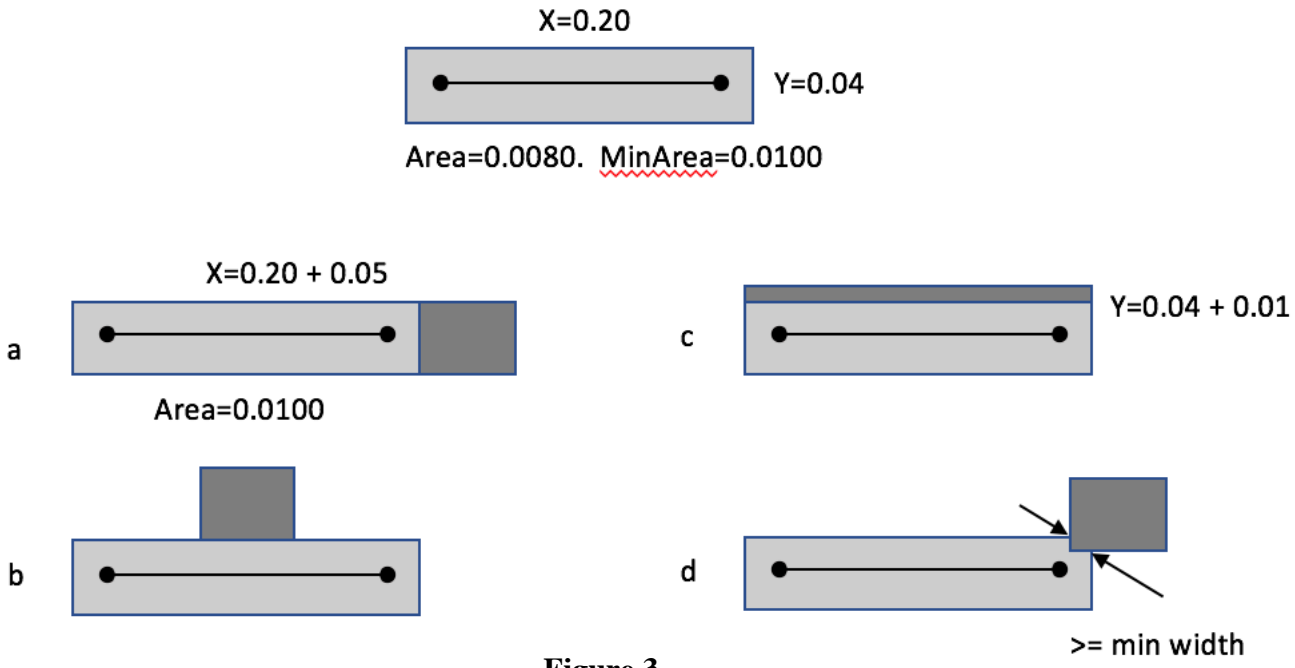


Figure 3

A patch metal is represented by the syntax "RECT (deltax1 deltay1 deltax2 deltay2)" in DEF file, which indicates that a rectangle is created from the previous (x y) routing point using the delta values. The RECT values leave the current point and layer unchanged. For example, in DEF file, a net "net123" has a patch metal (100, 100, 200, 200), which can be represented as "…(120, 110) RECT (-20, -10, 80, 90)".

Routing Preference Metrics

There are several metrics generally used to evaluate a detailed routing solution. Although they are not hard rules, the quality of a routing solution usually could be better in terms of timing, routability, manufacturability if the detailed router considers and optimizes these metrics.

1. Routing Guide Honoring

In the typical routing flow, global routing performs followed by detailed routing. A global routing result is usually well optimized for certain metrics (e.g., congestion, timing, skew, or slew), a detailed router needs to honor the global routing result as much as possible in order to minimize the disturbance to these metrics. In this contest, each benchmark has a *.guide file in which every net associates to a list of rectangles. The list of rectangles is called global routing guide to represent the regions passed by the global routing result of the associated net, and the global routing guide guarantees to cover at least a fully connected detailed routing solution for the net. If the center lines of wires or the coordinate of vias route outside of the guide, they will be considered as guide violations; if wires or vias route inside or just on the boundaries of the rectangles, there is no guide violation. In addition, routing guide honoring does not consider patch metals. Namely, patch metals can put out of guides without the penalty. For example, Figure 4(a) illustrates the guide representation in *.guide file for a net "net123" with two guide rectangles. Figure 4(b) shows a routing solution without guide violations, while Figure 4(c) shows a routing solution with guide violations for both via and wires. The score penalty will be applied based on the number of vias and the length of wires route out of guides.

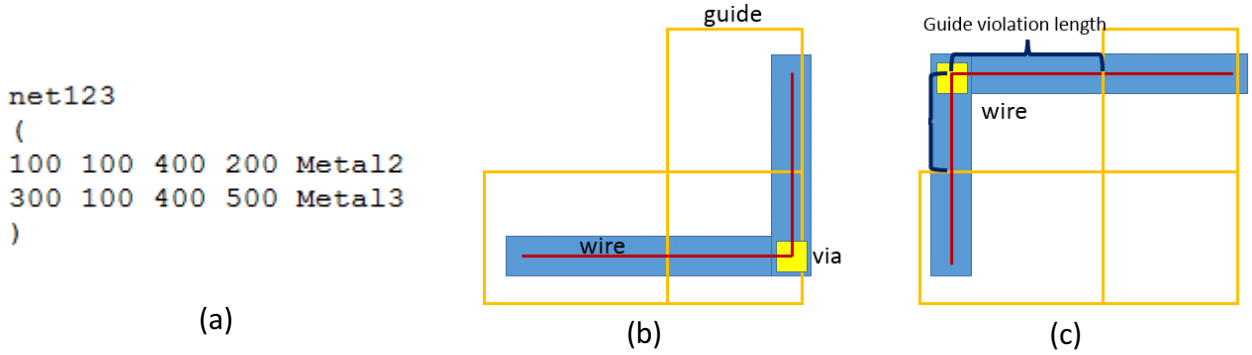


Figure 4

2. Wrong-way Routing

Each metal layer has a preferred routing direction defined by keyword "DIRECTION" in LEF file, which is either HORIZONTAL or VERTICAL. If a wire routes horizontally (vertically) on a vertical (horizontal) layer, the wire is considered as a wrong-way wire. The length of wrong-way wires will contribute the penalty to the scoring function.

3. Off-track Routing

Each metal layer has a track structure defined by keyword "TRACKS" in DEF files. The routing wires that align with tracks is so call on-track wires; otherwise, the wires are off-track wires. Also, a via is considered as an on-track via when the coordinate of the via aligns with the tracks on both its bottom and top layers. The length of off-track wires and the number of off-track vias will be considered as a penalty in the scoring function.

4. Multithreading Determinism

When technology nodes advance and design scale increases, the multithreading framework becomes an important feature to a detailed router. In this contest, we will evaluate the detailed routers on a machine with at least 8 CPUs, so multithreading implementation is encouraged but optional. (It is totally fine if the proposed detailed router uses only a single thread) However, multithreading technique is easier to have non-deterministic. Because non-deterministic behavior is a headache to debug and maintain a detailed router, it is better to avoid that. ***During solution evaluation stage, we will run the proposed detailed router multiple times with the fixed number of threads. If different runs for the same benchmark generate different results, the median result will be considered for the scoring and certain-level of the penalty will be applied to the score.*** The details of the machine status will be announced on 12/31/2017.

Summary

This contest will consider the following constraints/rules/metrics. Note that, the wirelength mentioned below does not include patch metals.

1. Number of open nets
2. Short metal area
3. Number of spacing violations (including spacing table, EOL, and cut spacing violations)
4. Number of min-area violations
5. Determinism
6. Total length of the wires outside of the routing guides
7. Total number of the vias outside of routing guides
8. Total length of off-track wires
9. Total number of off-track vias
10. Total length of wrong-way wires
11. Total length of wires
12. Total number of vias

In this contest, we will use Innovus to verify the detailed routing solutions and report the violations of connectivity and routing rules. The contest provides the document to introduce how to install Innovus and how to use Innovus to evaluate detailed routing solutions. Thus, the contestants can evaluate their detailed routing solution on their local servers. Then, we will provide an evaluation tool to read the violation reports from Innovus and consider the routing preference metrics for the given detailed routing solution to come out a score. The scoring function and the evaluation tool will be released by 12/31/2017.

The runtime of detailed routers will also be considered. There is a runtime factor that considers CPU time and real time to weight the score obtained by the evaluation tool. The contest ranking will be based on the weighted score. In addition, ***this contest will have max runtime and max memory usage constraints. If the usage of either runtime or memory is over a certain threshold for running a benchmark, the benchmark will be considered as a failure.*** More details will be announced by 12/31/2017.