ISPD 2019 Initial Detailed Routing Contest and Benchmarks with Advanced Routing Rules

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Organizers: Wen-Hao Liu, Stefanus Mantik, Wing-Kai Chow, Yixiao Ding, Amin Farshidi, Gracieli Posser

Cadence Design Systems
http://www.ispd.cc/contests/19/index.htm

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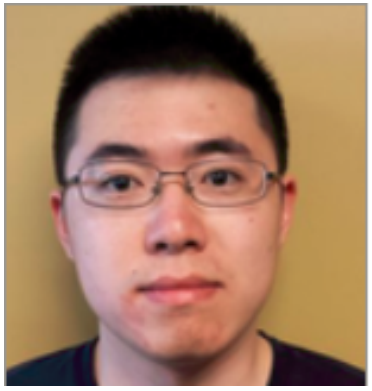
Contest Organizers

Gracieli Posser
Contest chair

Stefanus Mantik
Benchmarks



Yixiao Ding
Benchmark testing

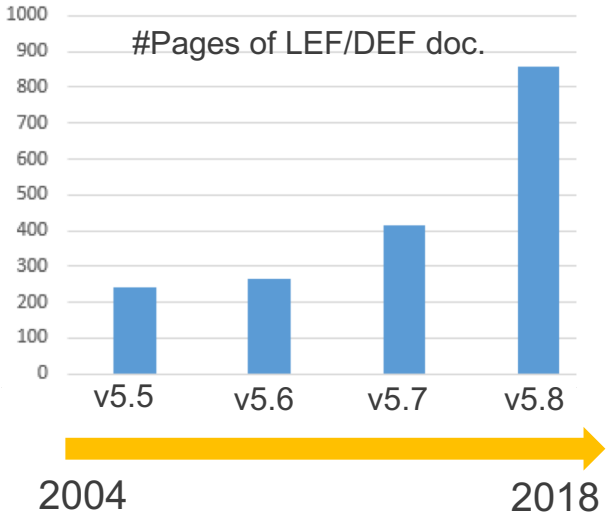
Amin Farshidi
Vice chair

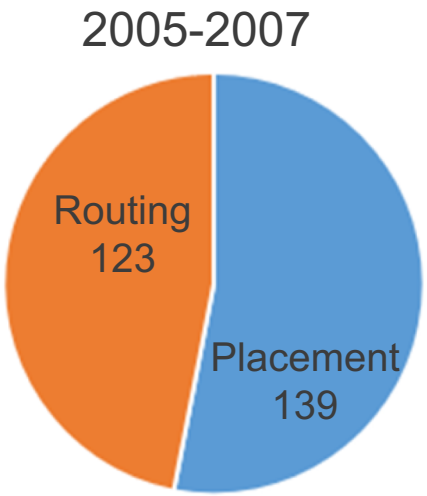
Wen-Hao Liu
Past chair

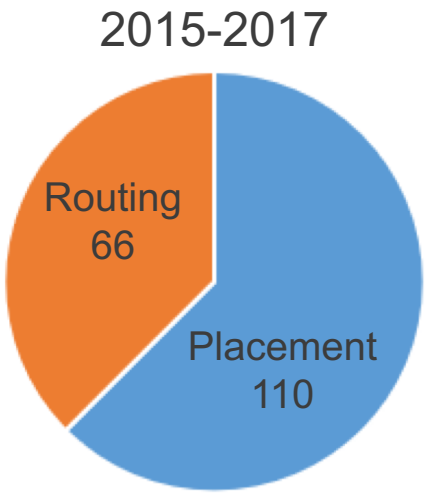
William Chow
Evaluation

Motivation

- Due to more and more complicated routing challenges, the demand for routing engineers is increasing from industry
- However, academia pay less attention to the routing field in recent years. There is shortage of graduated students with routing experience



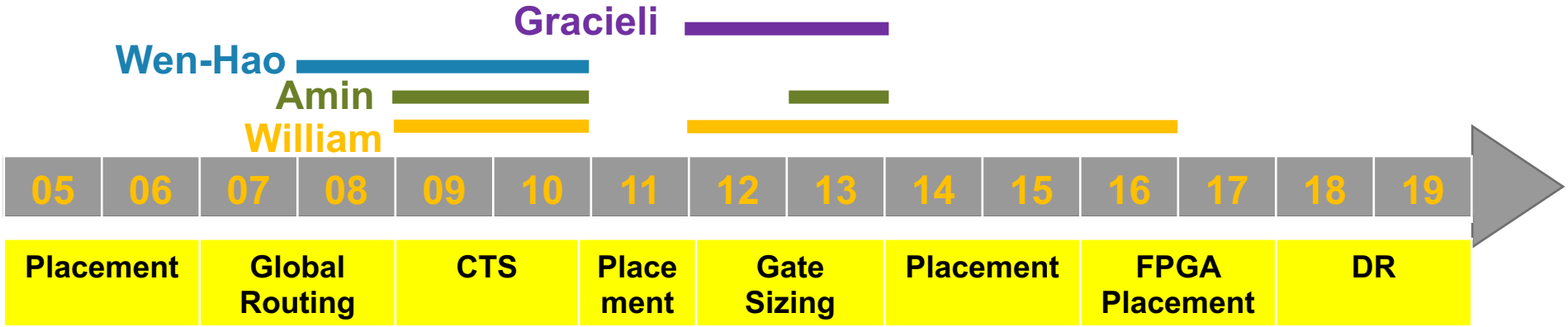




P&R paper count from DAC/ICCAD/ISPD/DATE/ASPDAC
Source: ACM Digital Library

Motivation

- Attract talent to address detailed routing challenges
- Drive practical detailed routing research to consider real design rules, memory scalability, and runtime scalability
- We learned a lot from the past contests, it is time to pay back to the community



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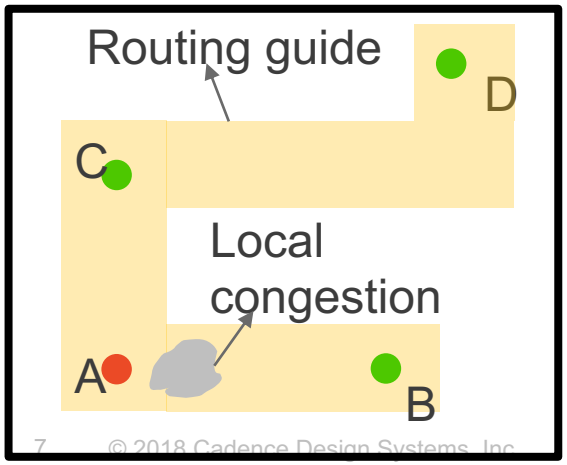
Outline

- Problem Introduction
- Benchmark Suite Characteristics
- Evaluation Metrics
- Contest Results
- Result Study
- Acknowledgements

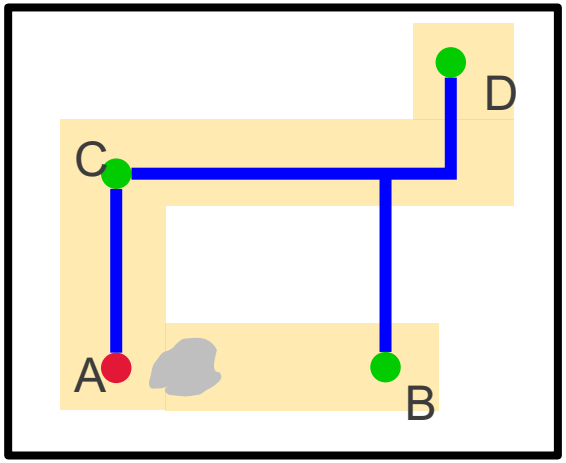
Problem Introduction

Initial Detailed Routing Problem

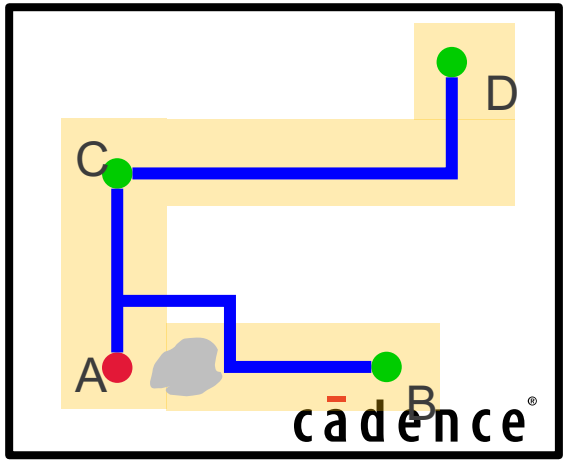
- Assuming that given routing guides are already well optimized for certain metrics, a detailed router needs to honor the guides as much as possible in order to keep the optimized metrics.
- If the initial detailed routing solution can meet the most common routing rules even it is not fully DRC clean, the later detailed routing refinement step will have less chance to largely disturb the routing solution.



Guide-violation solution



Guide-honoring solution

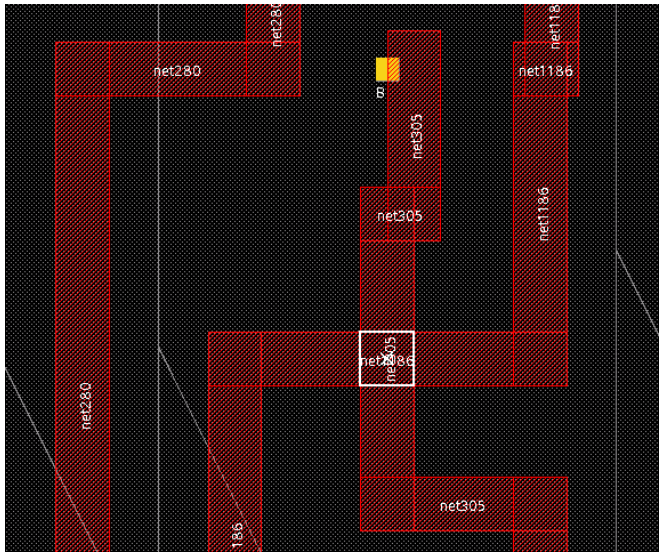


Open / Short

- Open: If any pin in a net is disconnected, the net will be considered as an open net and the routing solution is invalid.

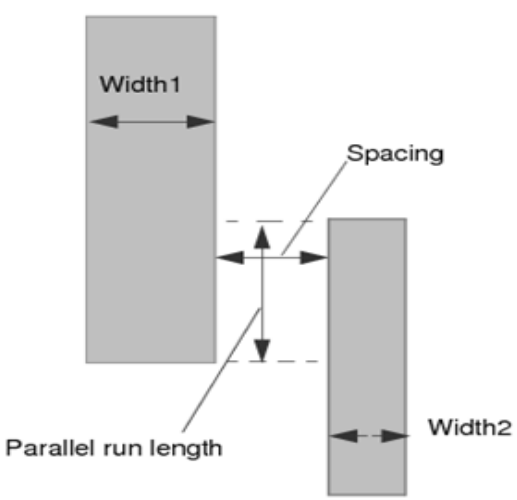
- Short: either a via metal or wire metal overlaps with another object like via metal, wire metal, blockages, or pin shapes.

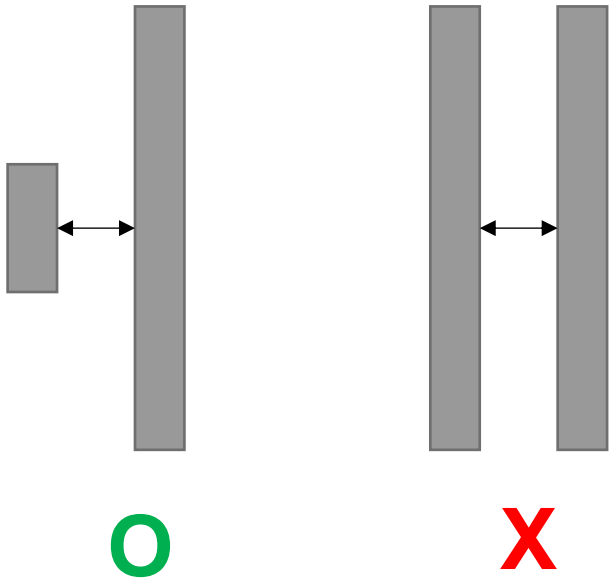
Short violation



Spacing Table

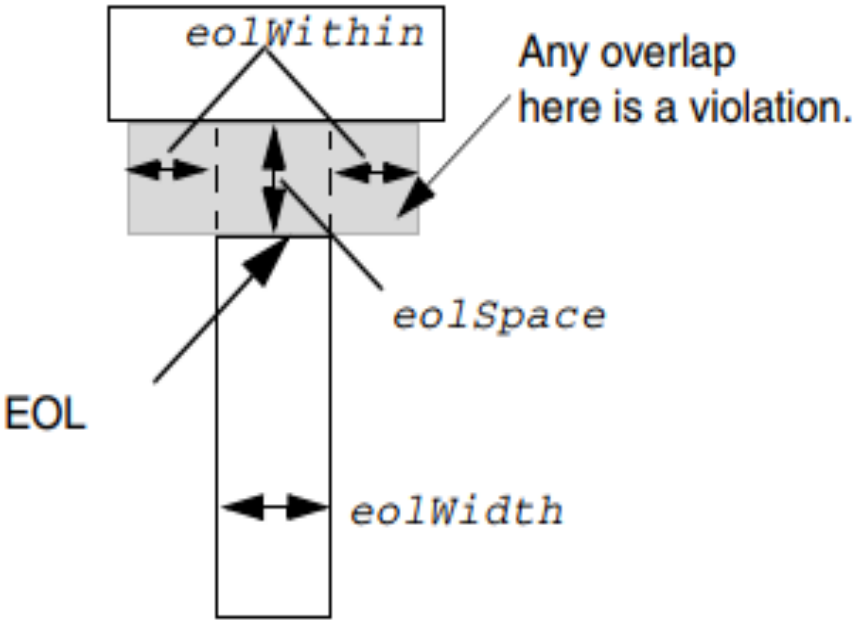
- Spacing table specifies the required spacing between two objects according to their parallel-run length and widths
- When two wires run in parallel for long distance, it may trigger bigger required spacing

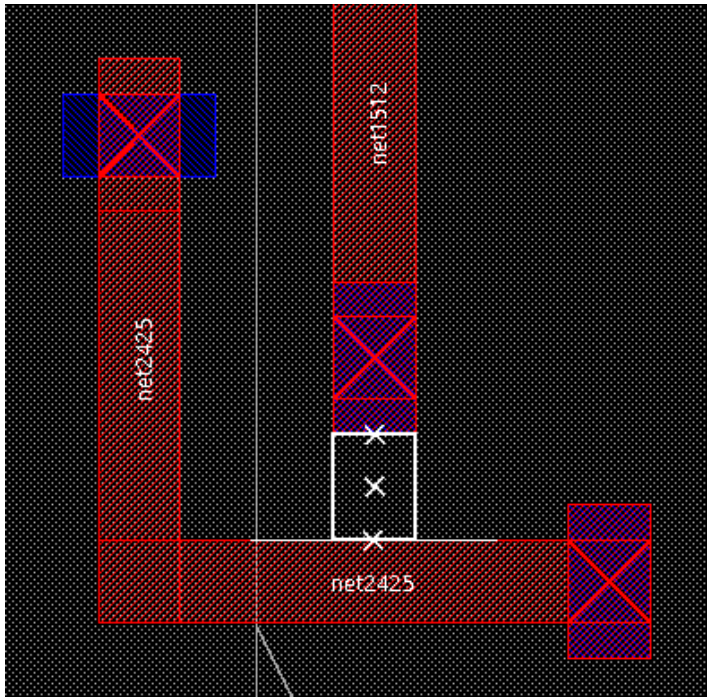




End of line (eol) spacing rule

- The end-of-line (EOL) spacing rule indicates that an edge that is shorter than *eolWidth*, noted as end-of-line edge requires spacing greater than or equal to *eolSpace* beyond the EOL anywhere within (that is, less than) *eolWithin* distance

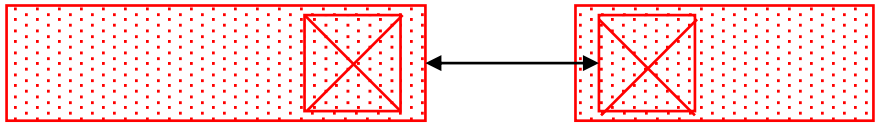




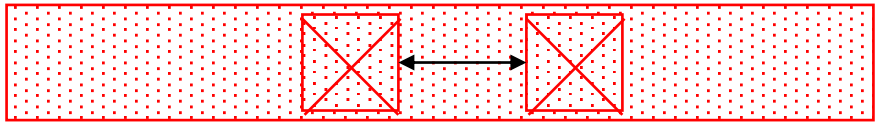
Cut Spacing

- A cut spacing specifies the minimum spacing between via cuts. It applies for cuts from both different nets and the same net.

- Stacked vias is allowed if their center are aligned.



Different net cut spacing

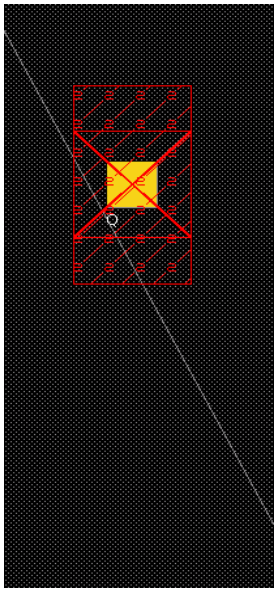


Same net cut spacing

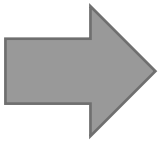
Min-Area Rule (MAR)

- The min area rule specifies the minimum metal area required for polygons on each layer. All polygons must have an area that is greater than or equal to the specified area value.

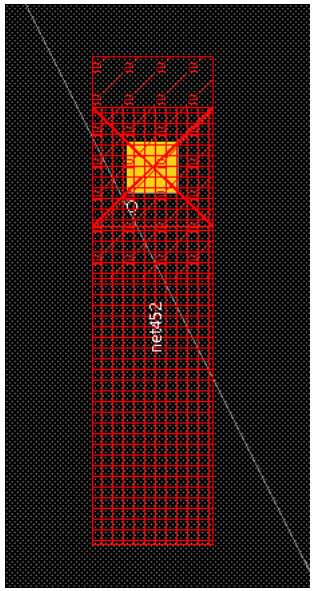
Min-area violation



Add patch wire

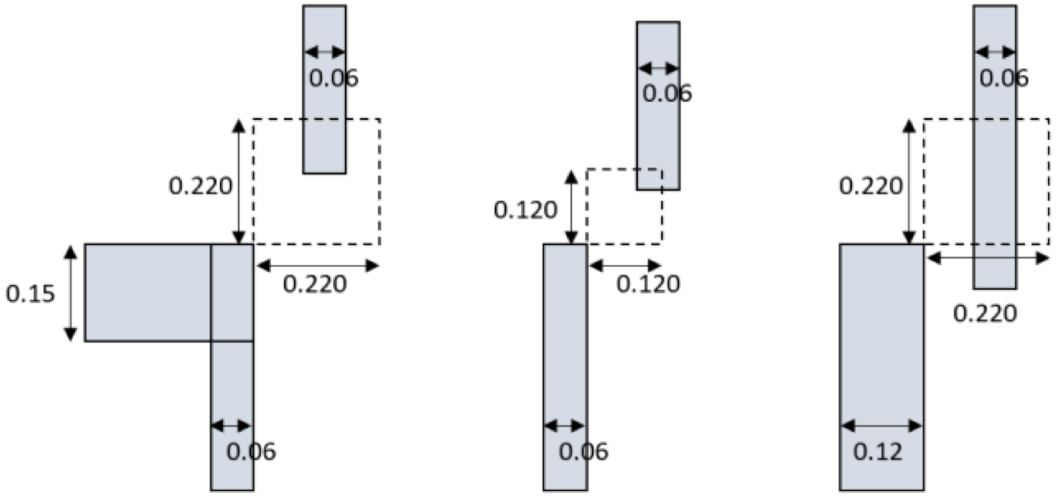


Min-area -violation-free



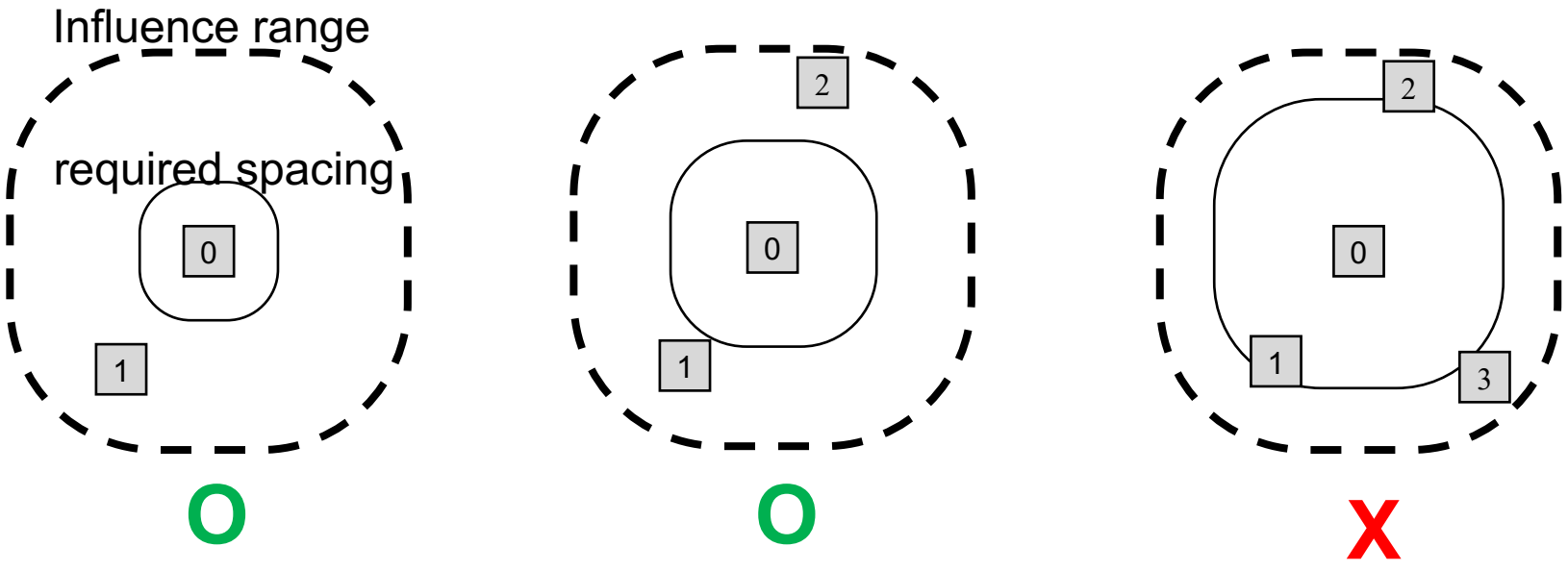
Corner-to-corner Spacing

- There are keep-out zones at the corners of each metal
- The size of the keep-out zone depends on the dimension of its associated metal
- If there is another metal's comer located in the keep-out zone, a violation happens



Adjacent Cut Spacing

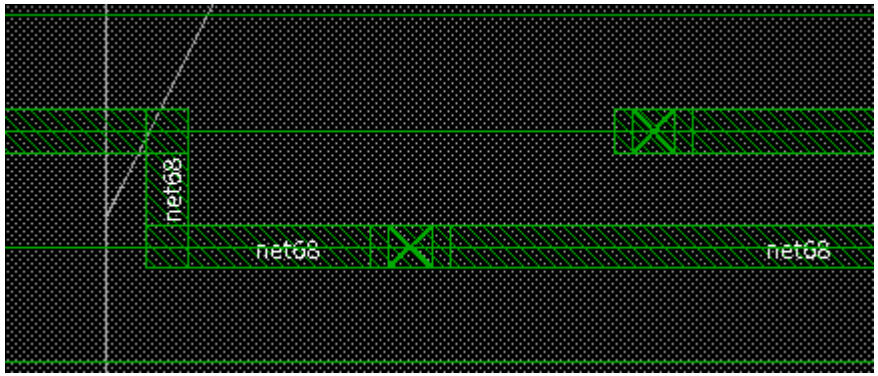
- Each via cut has an influence range
- If more cuts locate in a cut's influence range, the cut requires larger spacing away from other cuts

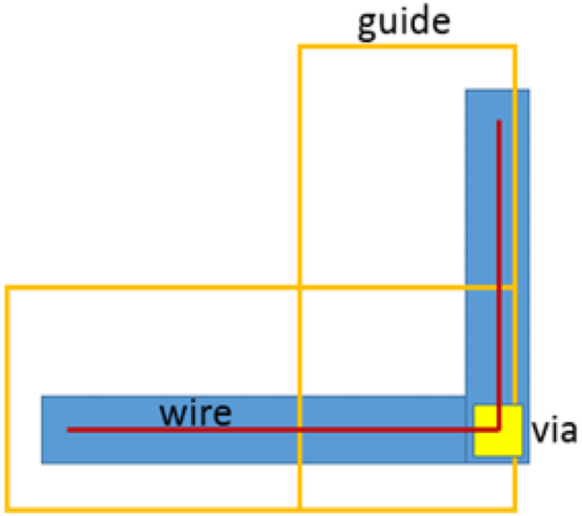


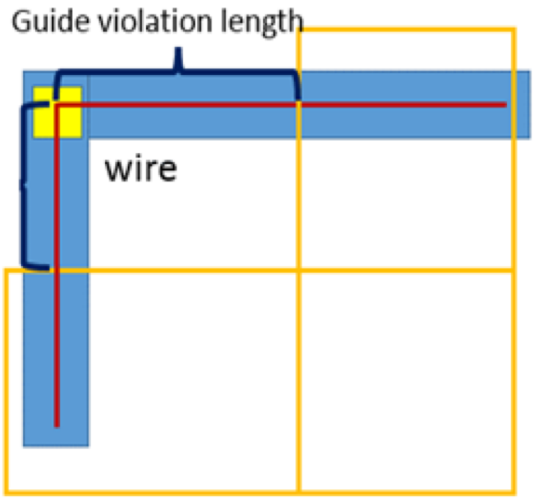
Routing Preference Metrics

- Wrong-way Routing
- Off-track Routing
- Routing Guide Honoring
- Non-determinism Penalty

Wrong-way routing







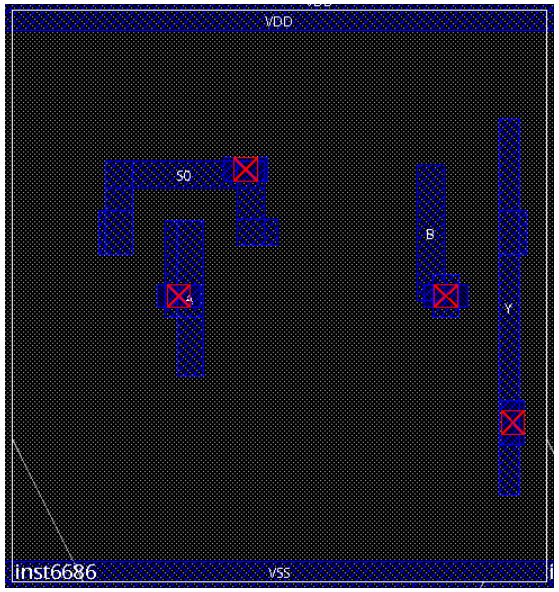
Double-cut via insertion

- For reality and performance concerns, detailed routers prefer to use double-cut vias rather than single-cut vias
- This contest encourages the usage of double-cut (D-cut) vias by making D-cut vias cheaper than single-cut vias during result evaluation

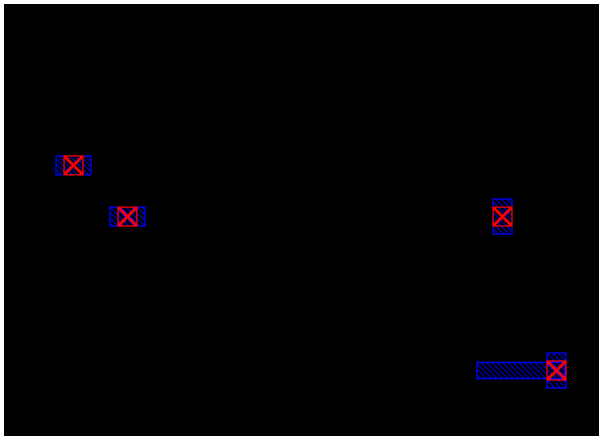
The challenges of this contest

- Pin-access location selection
- Via selection (D-cut via insertion)
- Patch wire insertion
- Memory and runtime controlling
  - Max runtime limit (vary by designs)
  - Max memory limit: 64GB

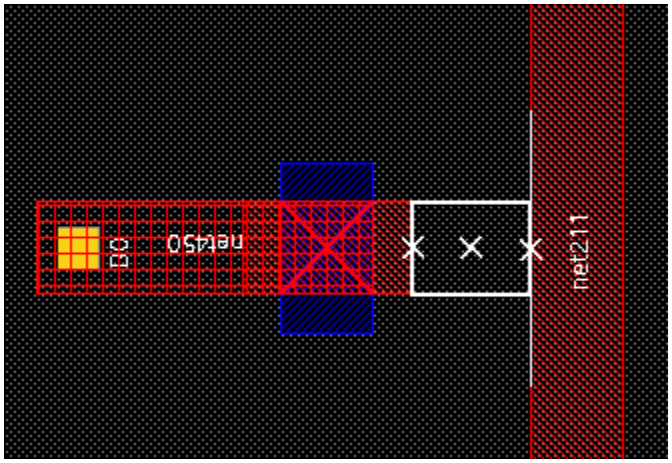
Pin access solution



Different vias



EOL-violation triggered by a patch



Benchmark Suite Characteristics

Benchmark Suite Characteristics

- The benchmarks are derived from two real designs (synthesized using generic 32nm cell library)
  - a single-core 32-bit processor with four memory cores
  - a quad-core 32-bit processor with 16 on-chip memory blocks
  - a DTMF design with three memory blocks and one PLL block
- Two designs are adapted from ISPD'15 test cases (uses 65nm cell library with rules modified for current contest)
  - mgc_matrix_mult_b
  - mgc_pci_bridge32_b
- Academic placer using the DATC RDF* methodology was used to place the cells on both ISPD'15 test cases (with an additional refine placement was added for mgc_pci_bridge32_b design)

*Jinwook Jung, et al., "DATC RDF: an academic flow from logic synthesis to detailed routing", *Proc. Intl. Conference on Computer-Aided Design* (ICCAD '18), ACM, Article 37.

Benchmark Suite Characteristics

- Simplifications for the contest
  - Non-default rules are removed
  - Timing related information are removed
- Power/Ground nets are present
- More realistic design rules
  - Full parallel-run-length spacing rule
  - Multiple EOL spacing rule
  - Corner-to-corner spacing rules
  - Adjacent cut rules in addition to a simple cut-to-cut spacing rule
- The routing for every benchmark can be done within 1 hour and 6 GB memory by using the commercial routers with eight threads.
- Every benchmark is guaranteed to have a DRC-violation-free solution

Benchmark Suite Characteristics

- Four small testcases with sample solutions are released early to enable the early development
- The final evaluation is based on 6 released and 4 hidden benchmarks

	#std	#blk	#net	#pin	#Layer	Die size
Sample testcases	ispd19_sample	22	0	11	0	9	0.017x0.010mm^2
	ispd19_sample2	22	1	16	0	9	0.017x0.010mm^2
	ispd19_sample3	5	1	7	5	16	1.900x2.000mm^2
	lspd19_sample4	67	0	22	0	9	0.195x0.195mm^2
Released benchmarks	ispd19_test1	8879	0	3153	0	9	0.148x0.146mm^2
	ispd19_test2	72094	4	72410	1211	9	0.873x0.589mm^2
	ispd19_test3	8283	4	8953	57	9	0.195x0.195mm^2
	ispd19_test4	146442	7	151612	4802	5	1.604x1.554mm^2
	ispd19_test6	179881	16	179863	1211	9	1.358x1.325mm^2
	ispd19_test9	899341	16	895253	3221	9	2.006x2.151mm^2
Hidden benchmarks	ispd19_test5	28920	6	29416	360	5	0.906x0.906mm^2
	ispd19_test7	359746	16	358720	2216	9	1.581x1.517mm^2
	ispd19_test8	539611	16	537577	3221	9	1.803x1.708mm^2
	ispd19_test10	899404	16	895253	3221	9	2.006x2.151mm^2

Summary of benchmark suite characteristics

ispd19_sample	45nm	Sample test for tutorial purpose
ispd19_sample2	45nm	Sample test with a block macro and nets connecting to the block
ispd19_sample3	45nm	Sample test that has IO pins and large design area
ispd19_sample4	32nm	Sample test that uses the 32nm library
ispd19_test1	32nm	Single-core design with standard cell only
ispd19_test2	32nm	Complete single-core design with four memory blocks
ispd19_test3	32nm	DTMF design with three memory blocks and one PLL block
ispd19_test4	65nm	ISPD'15 mgc_matrix_mult_b test case
ispd19_test6	32nm	Quad-core design with 16 memory blocks
ispd19_test9	32nm	Quad-core design with quadruple the number of standard cells and with 16 memory blocks
ispd19_test5	65nm	ISPD'15 mgc_pci_bridge32_b test case
ispd19_test7	32nm	Quad-core design with double the number of standard cells with 16 memory blocks
ispd19_test8	32nm	Quad-core design with triple the number of standard cells with 16 memory blocks
ispd19_test10	32nm	Quad-core design with quadruple the number of standard cells, with 16 memory blocks, and some extra routing blockages

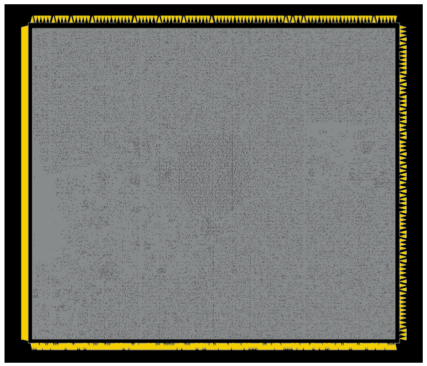
Comparing 2018 and 2019 Contest Benchmarks

- Biggest benchmark in 2018 and 2019 ISPD contests

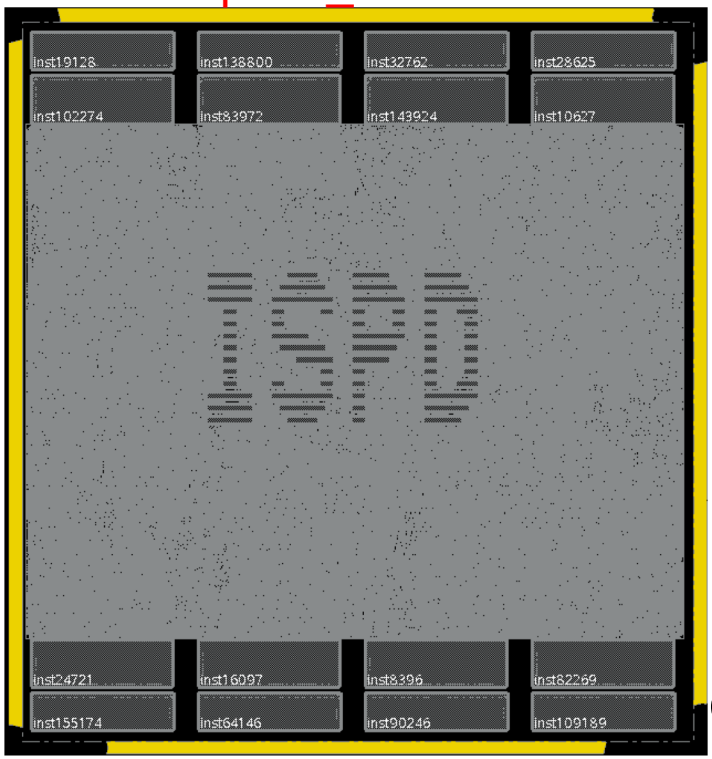
	#std	#blk	#net	#pin	#Layer	Die size
ispd18_test10	290386	0	182000	1211	9	0.910x0.780mm^2
ispd19_test10	899404	16	895253	3221	9	2.006x2.151mm^2

- Biggest benchmark this year is more than 4x bigger than the biggest one in 2018 ISPD contest

ispd18_test10

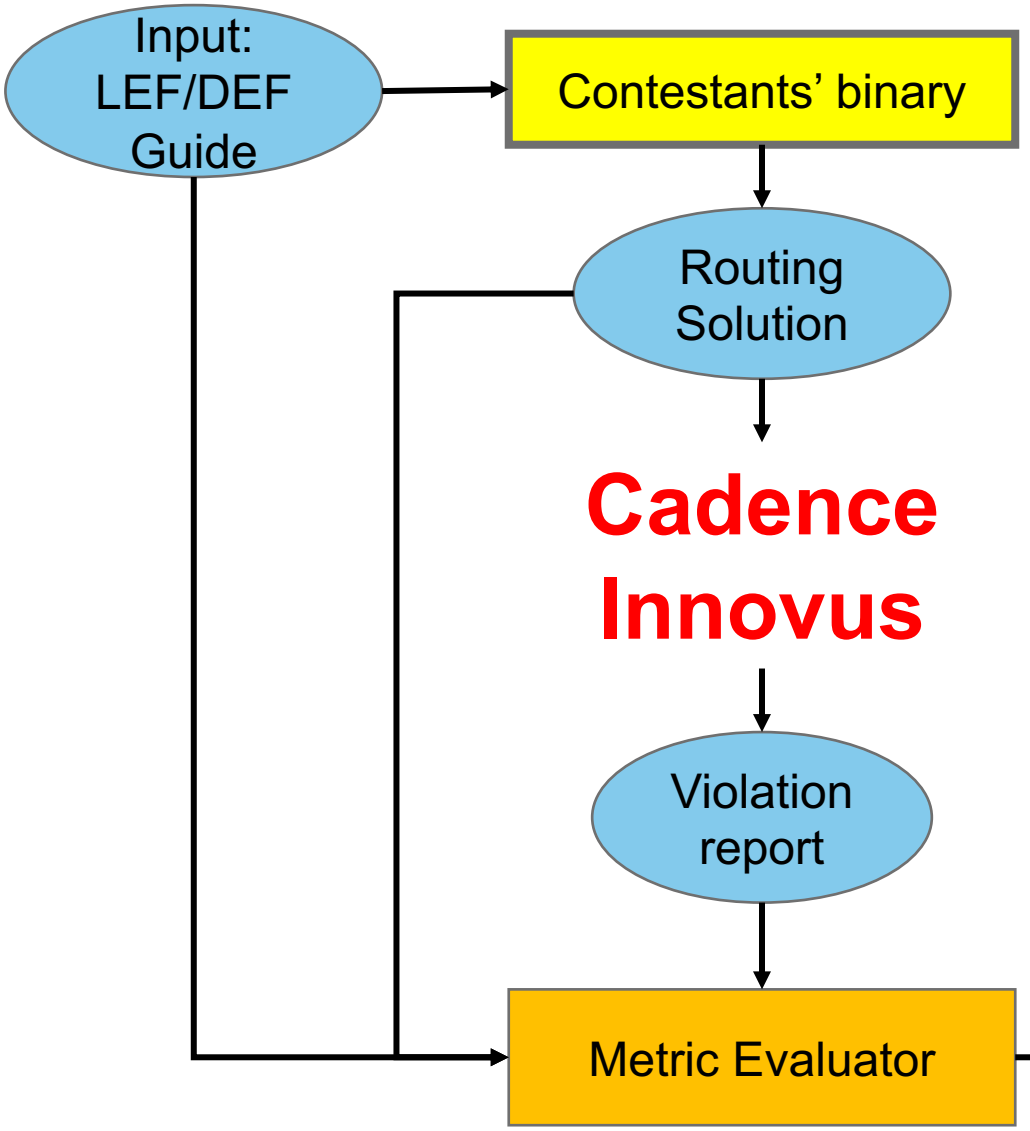


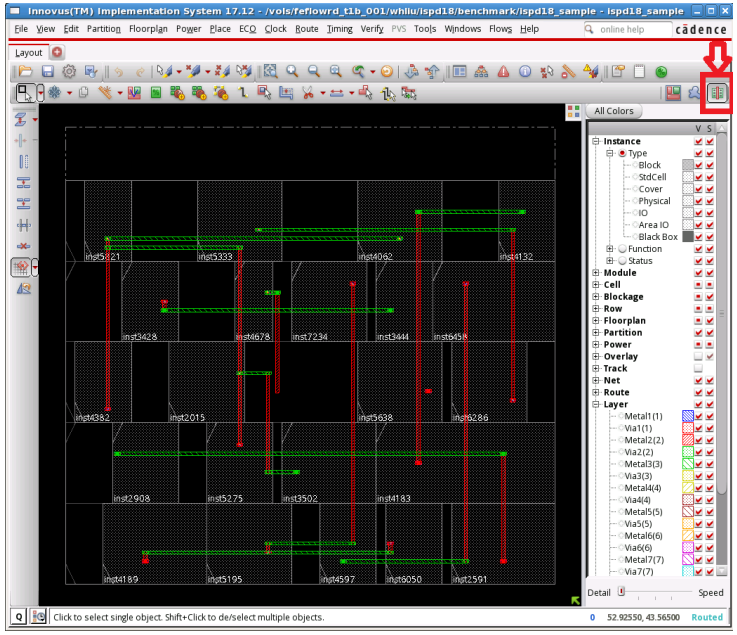
ispd19_test10



Evaluation

Evaluation Process





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Evaluation Metric

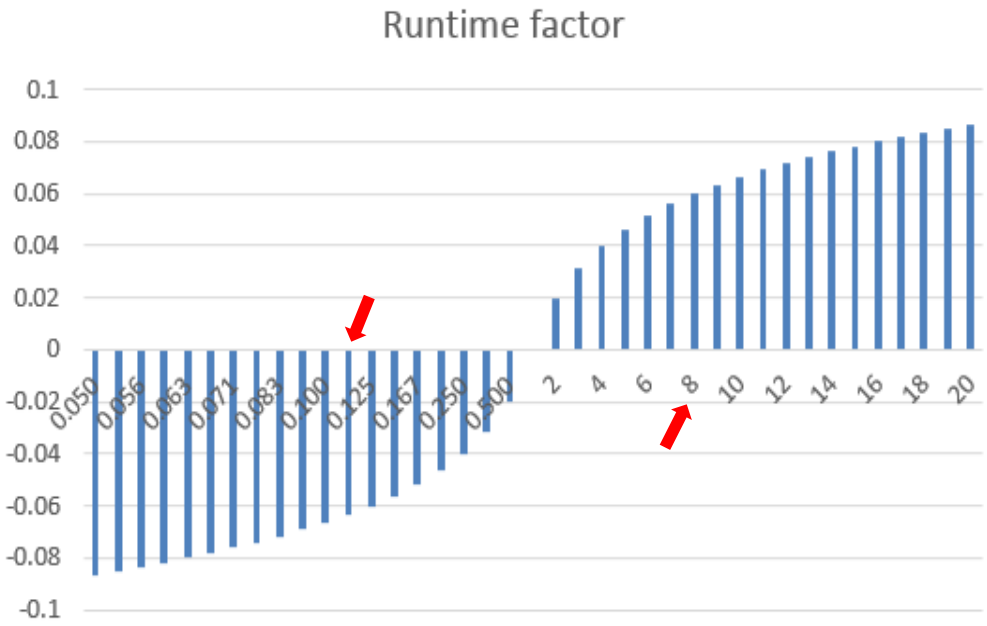
- The quality of result for a routing solution is measured by the following equation. A solution with a smaller scaled score is considered as a better solution in this contest
  - Scaled_score = raw_score * (1 + nondeterministic_penalty + runtime_factor)
- We will run each binary more than once. If we observe nondeterministic results, nondeterministic_penalty will be 3%; otherwise, it will be 0.

Metric	Weight
Total number of single-cut vias	4
Total number of multi-cut vias	2
Total length of wires	0.5
Out-of-guide wire length	1
Out-of-guide via count	1
Off-track wire length	0.5
Off-track via count	1
Wrong-way wire length	1

Metric	Weight
#short violations	500
Area of short violations	500
#end-of-line violations	500
#wire spacing violations	500
#via spacing violations	500
#corner spacing violations	500
#adjacent cut spacing violations	500
#min-area violations	500

Evaluation Metric (cont.)

- Runtime_factor = min(0.1, max(-0.1, **0.02 *** log2(**Router_Wall_Time / Median_Wall_Time**))
  - For each benchmark, we will select the “median_wall_time” based on the binary which can generate valid solutions.
  - Based on the following curve, say, a router is 8X faster/slower than the median, it will get 6% score benefit/penalty
  - The runtime penalty/benefit is limited within 10% and -10%



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Ranking Method

- Rank each team for each benchmark. The team with a smaller scaled score will get a smaller ranking number, which means a better ranking.
- Prune out the worst (i.e., biggest) ranking number, and then average the remaining rankings for each team. The team with the smallest averaged ranking number wins the contest.
- Example:

Scaled Score Table

	team 1	team 2	team 3	team 4	team 5
benchmark1	80	200	210	250	100
benchmark2	90	180	70	130	60
benchmark3	70	X	40	X	180
benchmark4	300	800	180	250	400
benchmark5	150	X	150	170	160

'X' means a failure

Ranking Table

	team 1	team 2	team 3	team 4	team 5
benchmark1	1	3	4	5	2
benchmark2	3	5	2	4	1
benchmark3	2	5 (X)	1	5 (X)	3
benchmark4	3	5	1	2	4
benchmark5	1	5 (X)	1	4	3

Final Ranking Result

	team 1	team 2	team 3	team 4	team 5
benchmark1	1	3	4	5	2
benchmark2	3	5	2	4	1
benchmark3	2	5	1	5	3
benchmark4	3	5	1	2	4
benchmark5	1	5	1	4	3
Avg without the outlier	1.75	4.5	**1.25**	3.75	2.25

Contest Results

Participation Statistics

- 33 initial registrations
  - Asia: 18 teams
  - North America: 8 teams (1 team cooperates with South America)
  - South America: 5 teams (1 team cooperates with North America)
  - Africa: 2 teams
  - Europe: 1 team
  - *Overall 9 different countries/regions*
  - *USA, China, Taiwan, Hong Kong, South Korea, Canada, Brazil, Sweden, Egypt*
- 9 alpha/beta binary submissions
- 7 final submissions

Participation Statistics

- 15 out of 33 teams did not participate last year contest
- 2 new teams are in the top-5
- We tried to promote ISPD contest in several different ways
- Thanks Cadence's support

ICCAD Invited Talk

University Tour

Cadence Press Release

Top 5 teams

- Top 5 teams will get plaques
- Top 3 teams will get cash reward sponsored by Cadence
  - 1st - $1500
  - 2nd - $1000
  - 3rd - $500

Team	Team name	Affiliation	Members
10	TripleZ	Fuzhou University and National Tsing Hua University	Zhen Zhuang, Chien-Hao Tsou, Weida Zhu, Chao-Yuan Huang, Genggeng Liu, Wenzhong Guo, Ting-Chi Wang
12	NTUidRoute	National Taiwan University	Chen-Chia Chang, Chia-Ming Chang, Wei-Kai Liu, Chen-Hao Hsu, Yao-Wen Chang
7	Kim & Lee	POSTECH	Daeyeon Kim, Sung-Yun Lee, Minhyuk Kweon, Seokhyeong Kang
15	Dr. CU	The Chinese University of Hong Kong	Gengjie Chen, Haocheng Li, Bentian Jiang, Jingsong Chen, Evangeline Young
1	SmartDR	Universidade Federal de Pelotas	Stephano Gonçalves, Felipe Marques

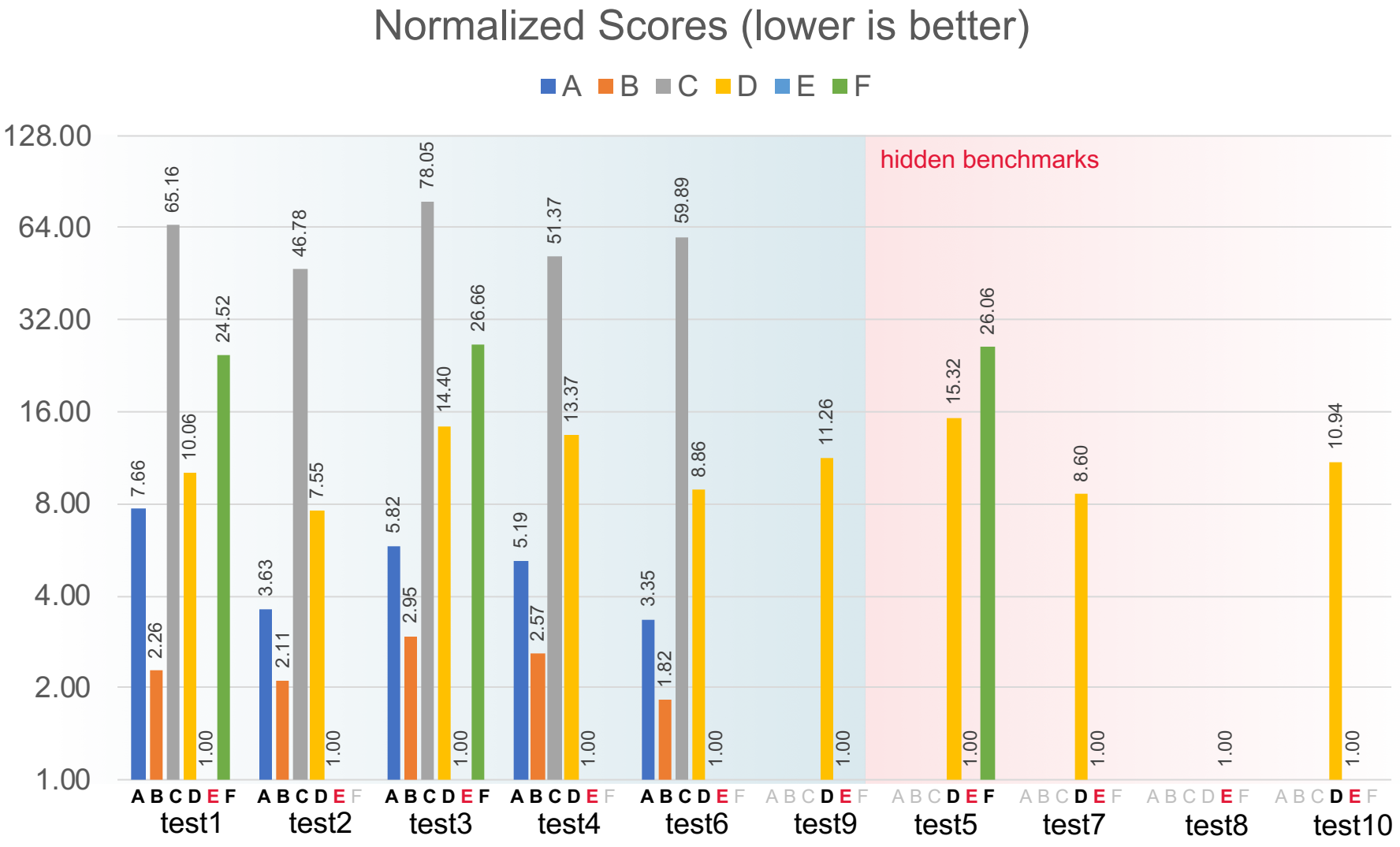
Result Overview

- Open nets comparison
  - No solution is considered as all nets open

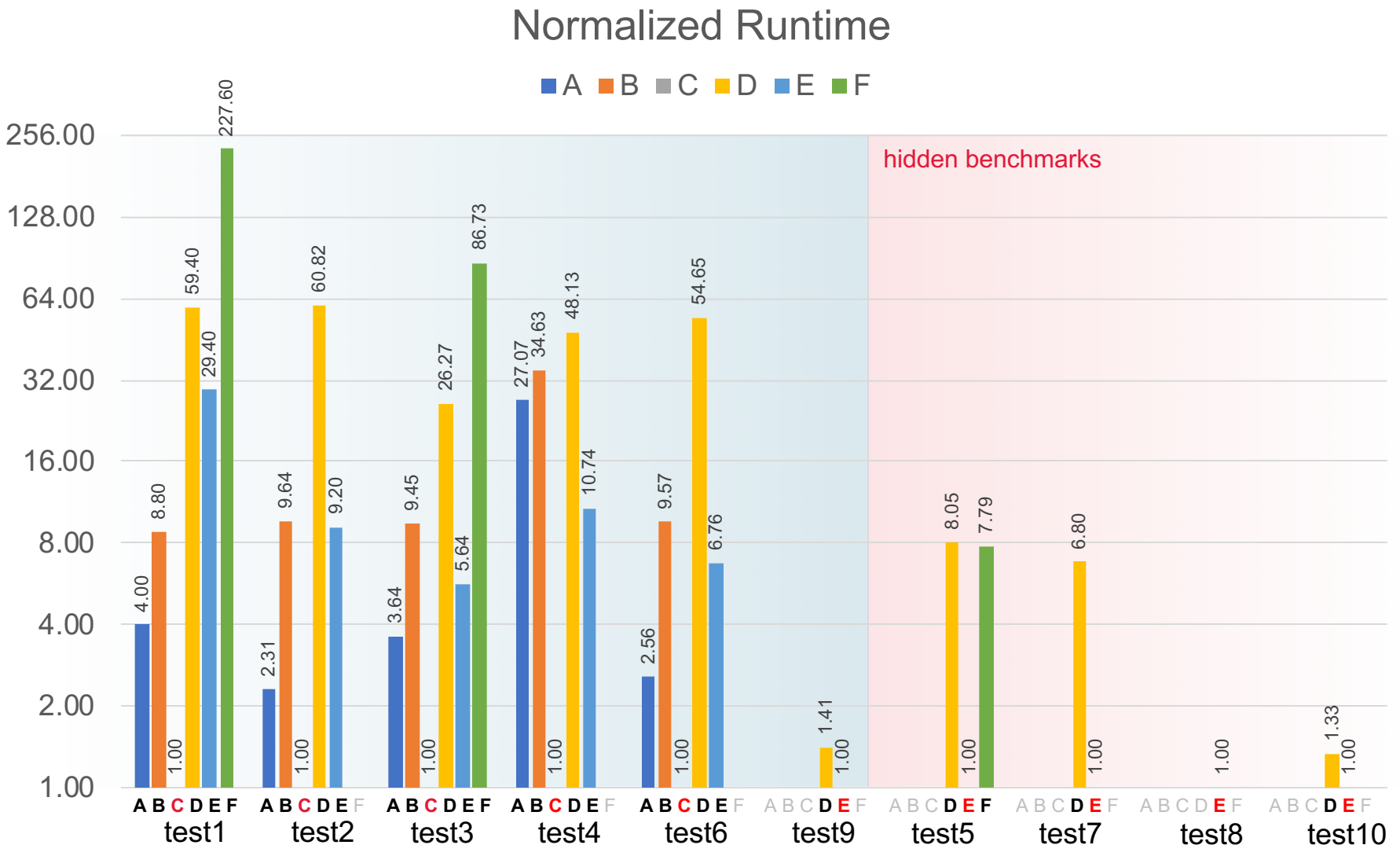
Mem : out-of-memory
Time : over time limit
No sol : no solution at exit

		A	B	C	D	E	F	G
	test1	0	0	0	0	0	0	Time
	test2	0	0	0	0	0	No sol	Time
	test3	0	0	0	0	0	0	Time
	test4	0	0	0	0	0	No sol	Time
hidden	test5	No sol	29416	3	0	0	0	Time
	test6	0	0	0	0	0	No sol	Time
hidden	test7	No sol	Mem	21	0	0	Mem	Time
hidden	test8	No sol	Mem	12	No sol	0	Mem	Mem
	test9	No sol	Mem	18	0	0	Mem	No sol
hidden	test10	No sol	Mem	25	0	0	Mem	No sol

Result Overview



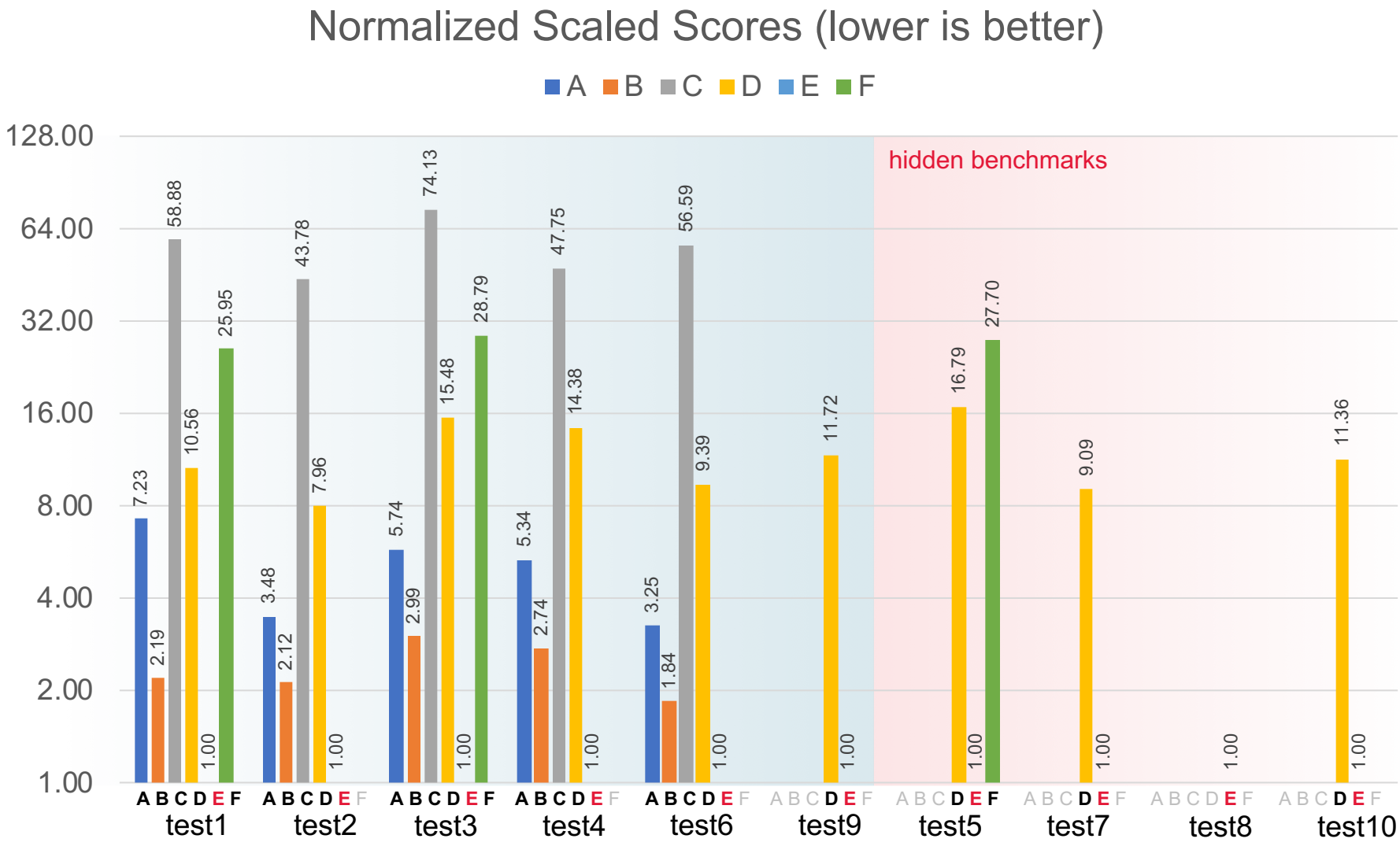
Result Overview



cadence

Result Overview

- Scaled scores considering run-time factor



cadence

Result Overview

- Final ranking

Normalized scaled scores

	A	B	C	D	E	F	G
test1	7.2	2.2	58.9	10.6	1.0	26.0	
test2	3.5	2.1	43.8	8.0	1.0		
test3	5.5	3.0	74.1	15.5	1.0	28.8	
test4	5.3	2.7	47.8	14.4	1.0		
test5				16.8	1.0	27.7	
test6	3.3	1.8	56.6	9.4	1.0		
test7				9.1	1.0		
test8					1.0		
test9				11.7	1.0		
test10				11.4	1.0		

Ranking

	A	B	C	D	E	F	G
test1	3	2	6	4	1	5	7
test2	3	2	5	4	1	7	7
test3	3	2	~~6~~	4	1	5	7
test4	3	2	5	4	1	7	7
test5	7	5	4	2	1	3	7
test6	3	2	5	4	1	7	7
test7	7	7	3	2	1	7	7
test8	7	7	2	~~7~~	1	7	7
test9	7	7	3	2	1	7	7
test10	~~7~~	~~7~~	3	2	~~1~~	~~7~~	~~7~~
	4.8	**4**	**4**	**3.1**	**1**	**6.1**	**7**

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Fifth Place

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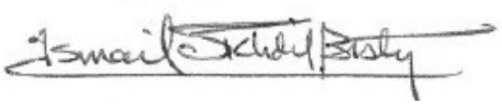
2019 ACM International Symposium on Physical Design

Initial Detailed Routing Contest

Universidade Federal de Pelotas

SmartDR

Stephano Gonçalves, Felipe Marques



Ismail Bustany
General Chair

William Swartz
Technical Program Chair

Gracieli Posser
Contest Chair


Fourth Place


Third Places

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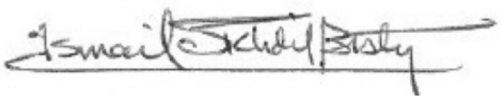
Initial Detailed Routing Contest

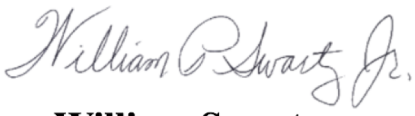
POSTECH

Kim & Lee

Daeyeon Kim, Sung-Yun Lee, Minhyuk Kweon, Seokhyeong Kang



Ismail Bustany
General Chair



William Swartz
Technical Program Chair

Gracieli Posser
Contest Chair

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Initial Detailed Routing Contest

Fuzhou University and National Tsing Hua University

TripleZ

Zhen Zhuang, Chien-Hao Tsou, Weida Zhu, Chao-Yuan Huang, Genggeng Liu, Wenzhong Guo, Ting-Chi Wang

Ismail Bustany
General Chair

William Swartz
Technical Program Chair

Gracieli Posser
Contest Chair


Second Place

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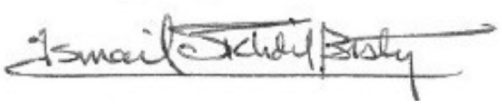
Initial Detailed Routing Contest

National Taiwan University

NTUidRoute

Chen-Chia Chang, Chia-Ming Chang, Wei-Kai Liu,
Chen-Hao Hsu, Yao-Wen Chang



Ismail Bustany
General Chair

William Swartz
Technical Program Chair

Gracieli Posser
Contest Chair


First Place

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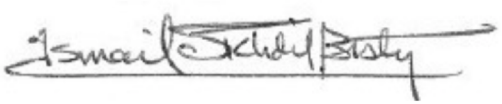
2019 ACM International Symposium on Physical Design

Initial Detailed Routing Contest

The Chinese University of Hong Kong

Dr. CU

Gengjie Chen, Haocheng Li, Bentian Jiang, Jingsong Chen, Evangeline Young



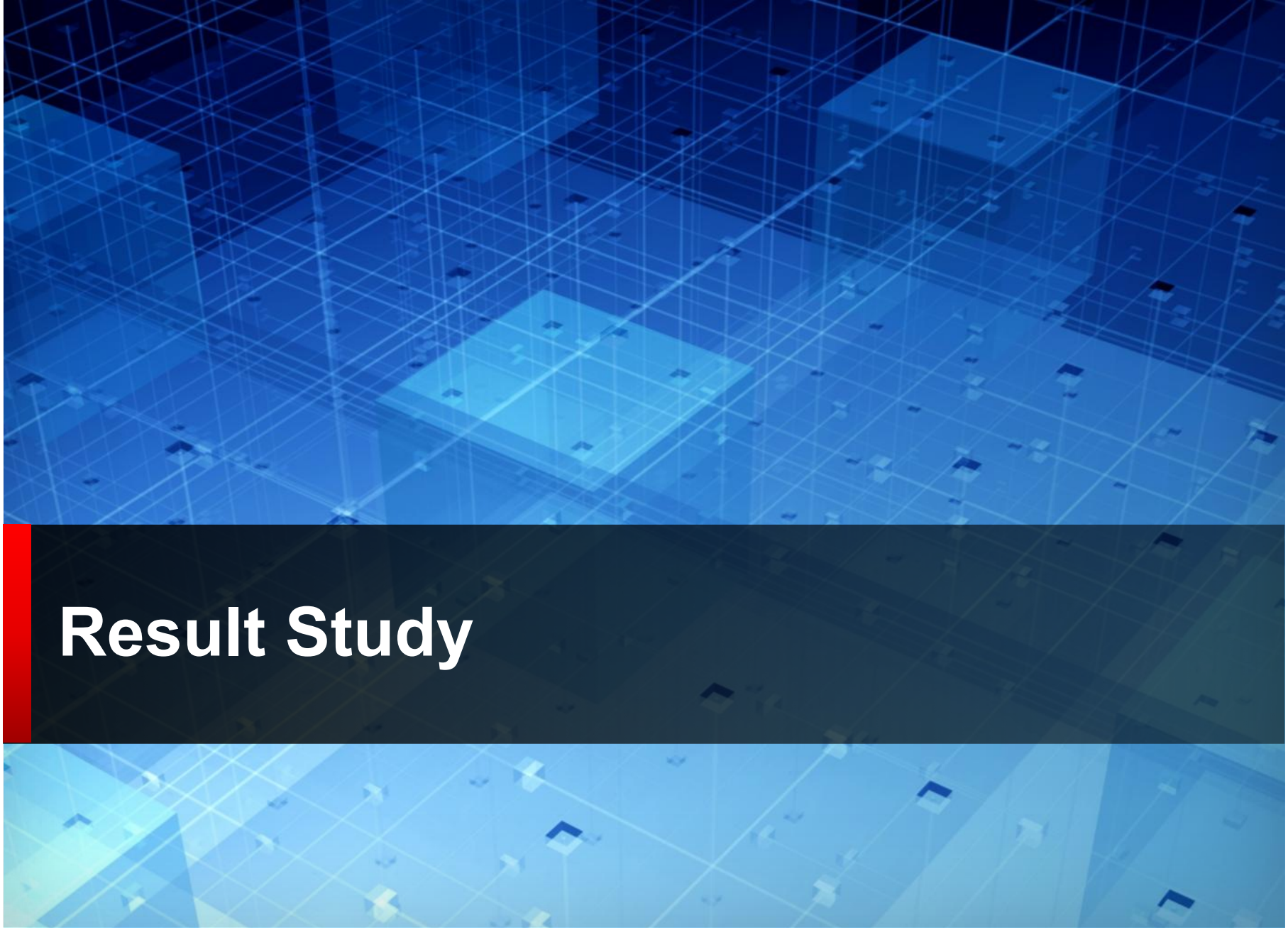
Ismail Bustany
General Chair

William Swartz
Technical Program Chair

Gracieli Posser
Contest Chair

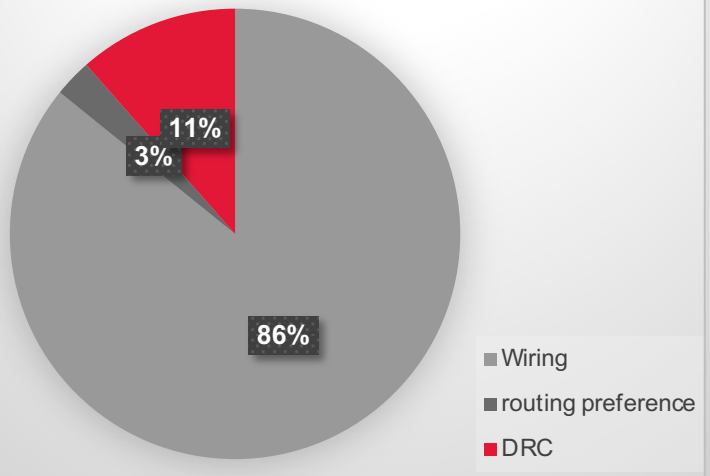
Ranking Announcement

- 1st Place:
  - Dr. CU (The Chinese University of Hong Kong)
- 2nd Place
  - NTUidRoute (National Taiwan University)
- 3rd Place:
  - Kim & Lee (POSTECH)
  - TripleZ (Fuzhou University and National Tsing Hua University)
- 5th Place:
  - SmartDR (Universidade Federal de Pelotas)

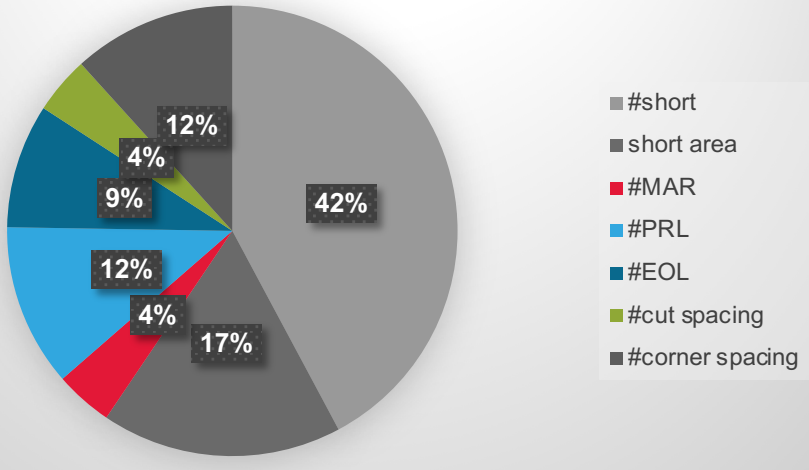


Result Study

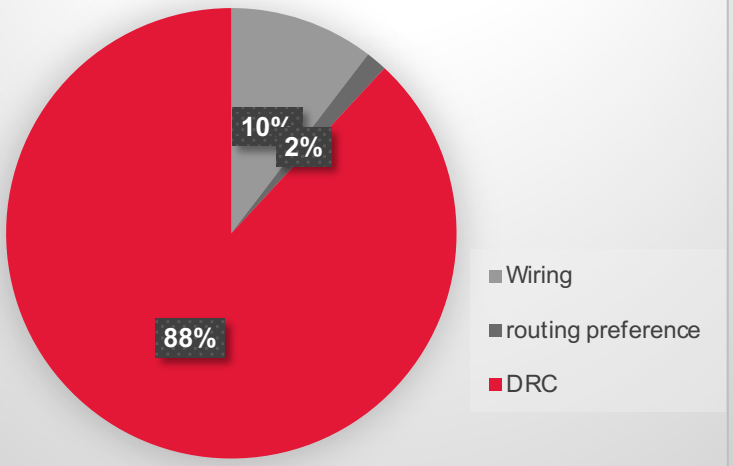
Dr. CU score breakdown on test6



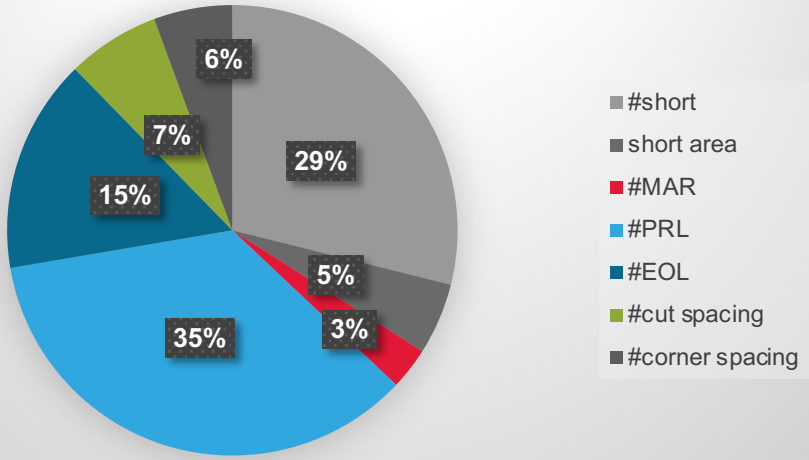
DRC score breakdown on test6



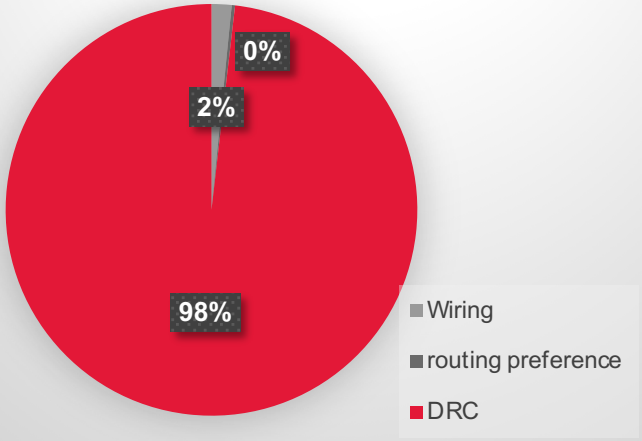
NTUidRoute score breakdown on test6



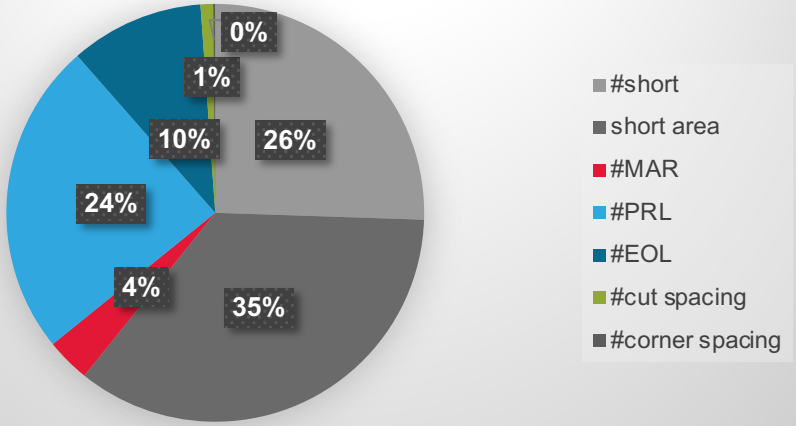
DRC score breakdown on test6



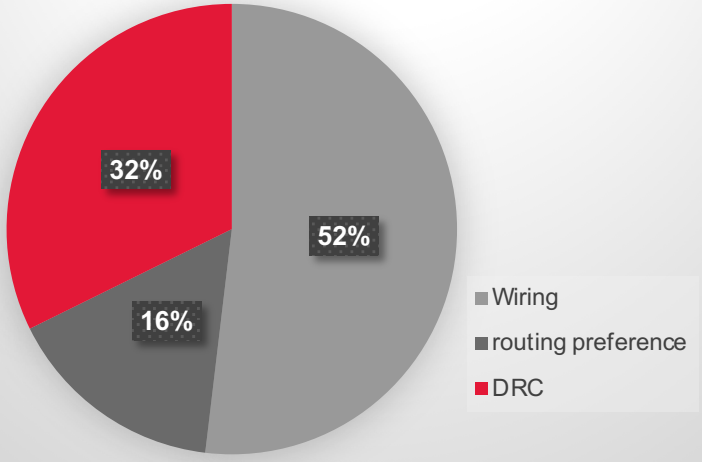
TripleZ score breakdown on test6



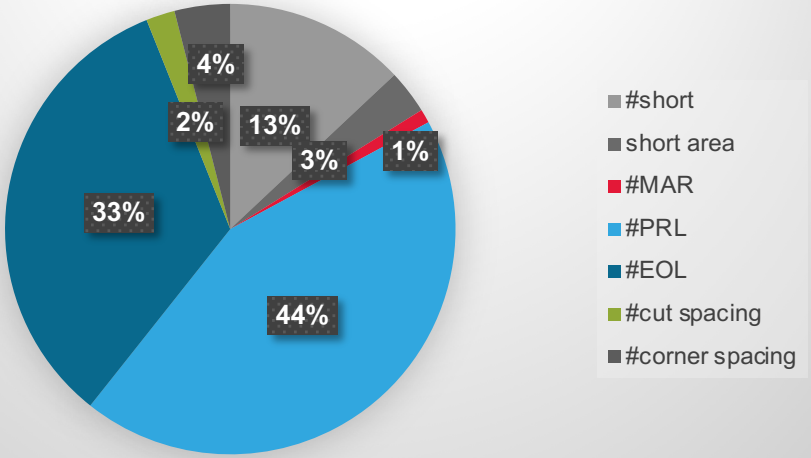
DRC score breakdown on test6



Kim & Lee score breakdown on test6



DRC score breakdown on test6



Wire Length (WL) and Number of Vias (test6)

Dr. CU

- Lowest total WL

NTUidRoute

- Highest WL on Metal 9

Kim & Lee

- Lowest number of vias and WL on Metal1 (this will help pin access)

TripleZ

- Highest total WL
- Lowest total number of vias

Wire Length

	Dr. CU	NTUidRoute	Kim & Lee	TripleZ
Metal1	43038092	92929020	15176846	180566241
Metal2	3031689863	3075793700	1832000182	4311174623
Metal3	4479301059	4237577650	4416428030	4643089485
Metal4	2875490575	3047570610	4254001900	2927356759
Metal5	1010148725	1312743760	1232234240	1089977550
Metal6	413207864	450478550	525561494	594015346
Metal7	698072570	712175130	707543716	644739420
Metal8	655226086	730267240	658713280	489387720
Metal9	12340800	58130800	19259600	50739050
Total	**13218515634**	**13718213150**	**13661397689**	**14931046194**

# of vias

	Dr. CU	NTUidRoute	Kim & Lee	TripleZ
Metal1	825819	899852	790098	982624
Metal2	1038965	1211723	1104345	805435
Metal3	119704	285415	642728	113125
Metal4	15027	24118	135201	15137
Metal5	4314	5939	32631	5752
Metal6	4355	5415	7052	4344
Metal7	2300	3412	3530	2314
Metal8	233	694	955	337
Total	**2010717**	**2436568**	**2716527**	**1929068**

Multi-Cut Vias and Violation Count (test6)

	Dr. CU	NTUidRoute	Kim & Lee	TripleZ
# multi-cut vias	0	269	0	2314
# cut spacing viols	453	49838	1174	54303
# adjacent cut spacing viols	69	2582	957	693
# parallel run length viols	1283	263404	24343	1371765
# corner to corner spacing viols	1288	42010	2229	9431

Dr. CU

- No multi-cut vias
- Lowest number of violations

NTUidRoute

- Highest number of adjacent cut spacing and corner to corner spacing violations

Kim & Lee

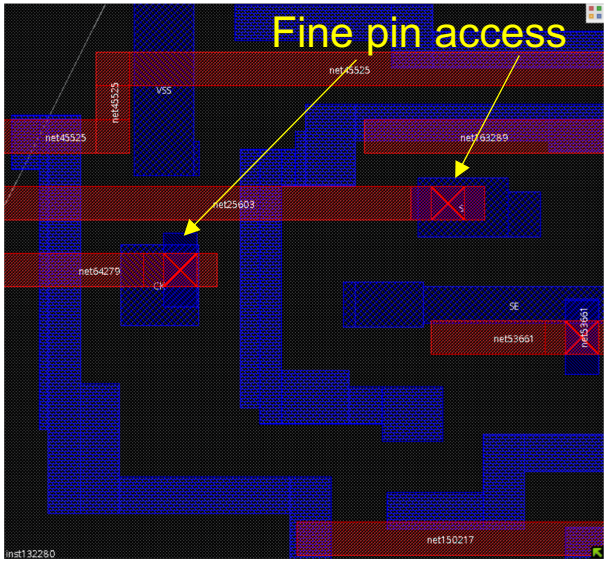
- No multi-cut vias

TripleZ

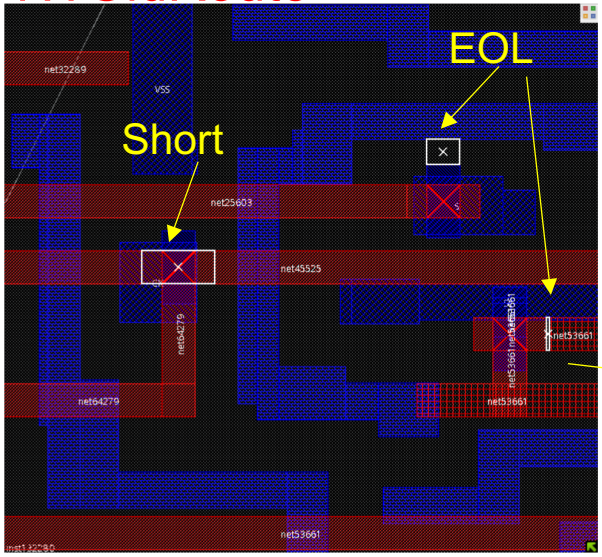
- Highest number of multi-cut vias
- Highest number of cut spacing and parallel run length violations

Pin access

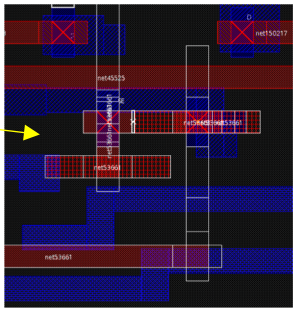
Dr. CU



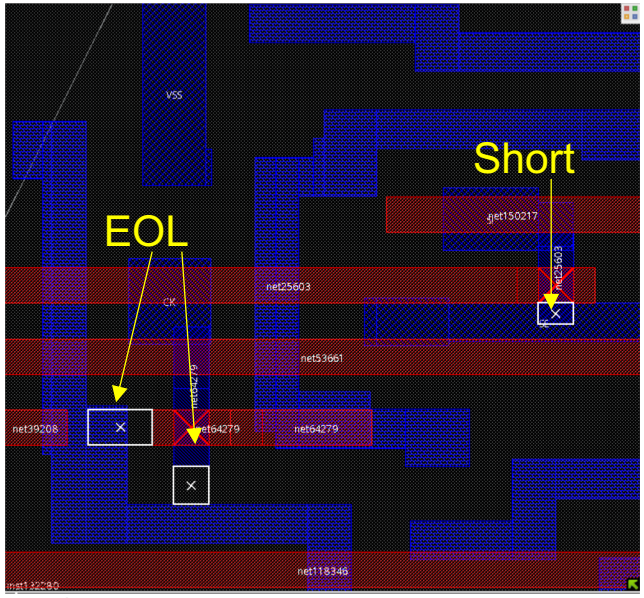
NTUidRoute



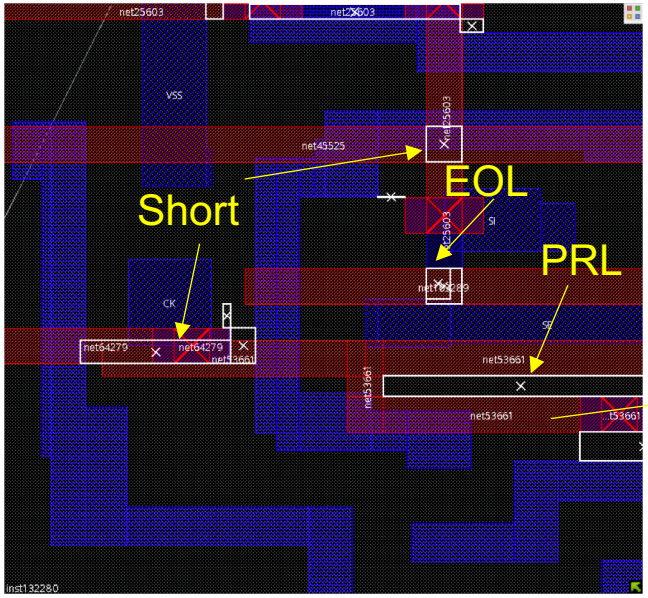
Detour for pin access



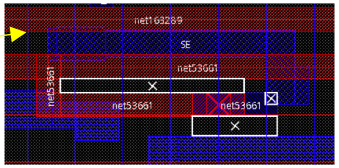
Kim & Lee



TripleZ

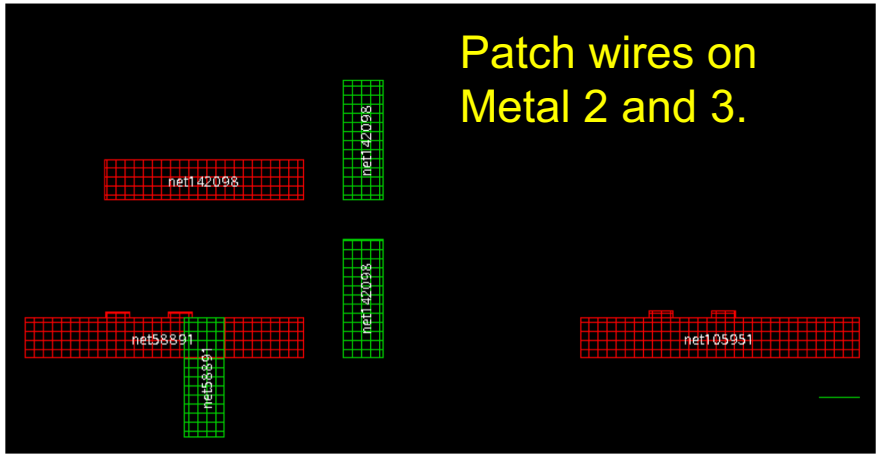


Detour and violations for pin access. Pins are off track.

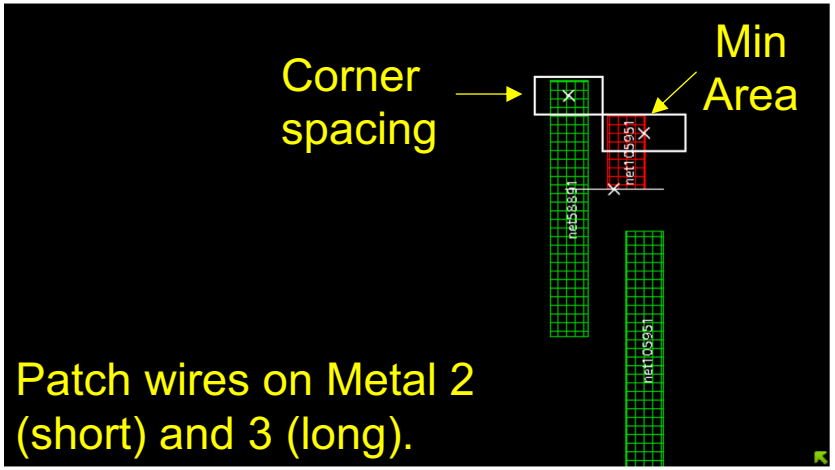


Patch Wires

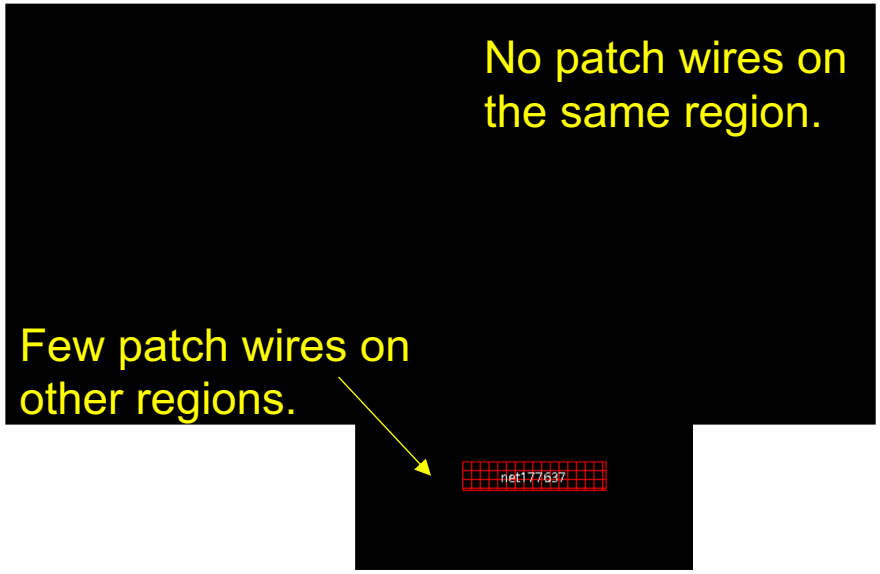
Dr. CU



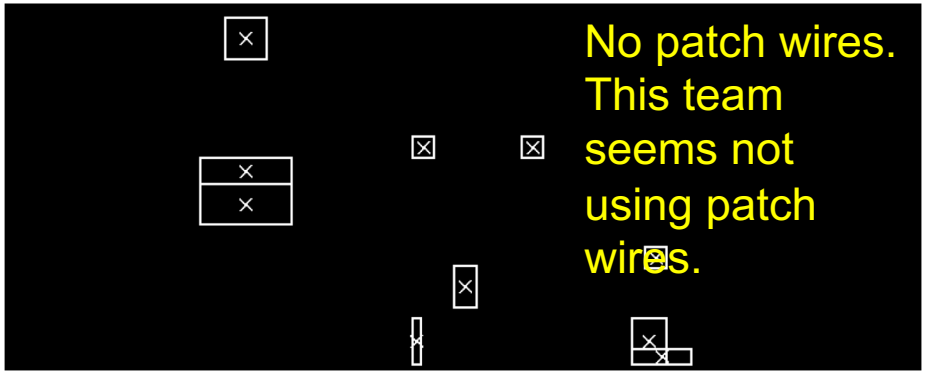
NTUidRoute



Kim & Lee

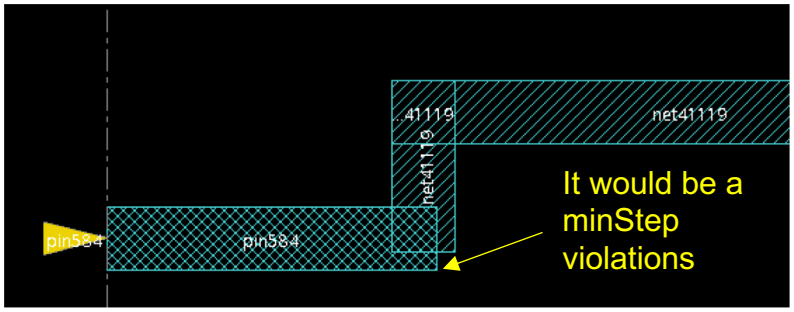


TripleZ



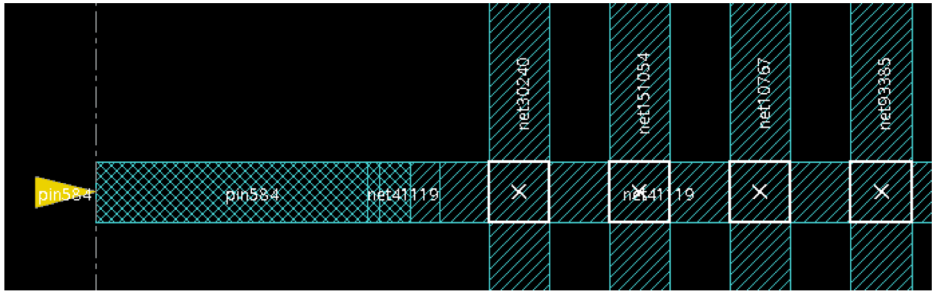
Wrong way routing

Dr. CU



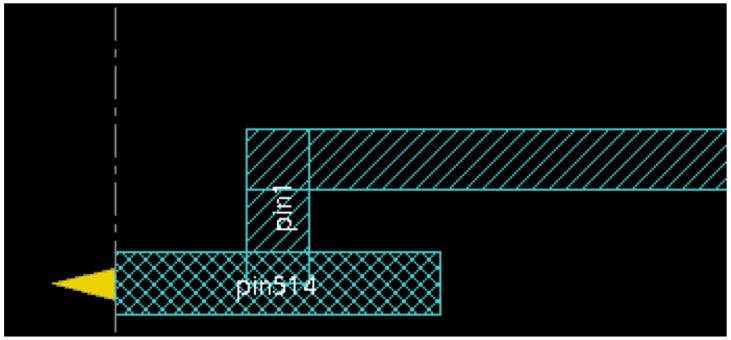
Metal8 (H) IO pin connection and wrong way routing

NTUidRoute



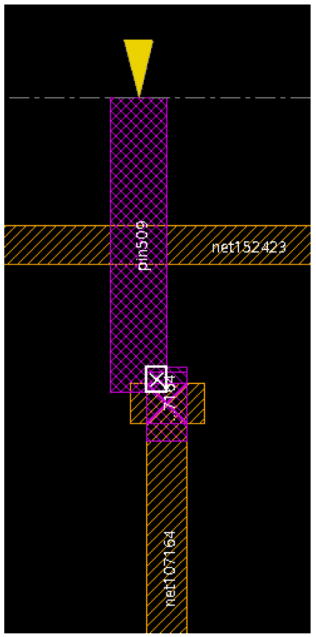
Metal8 (H) IO pin connection. Shorts with other nets with wrong way routing.

Kim & Lee



Metal8 (H) IO pin connection and wrong way routing

TripleZ

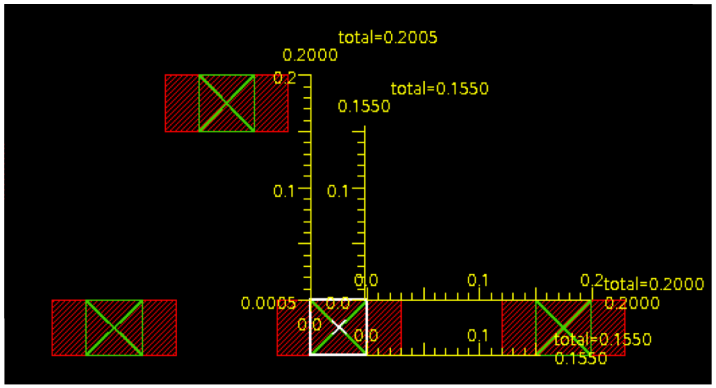


Metal6 (H) IO pin connection and wrong way routing. Non-sufficient metal violation

cadence

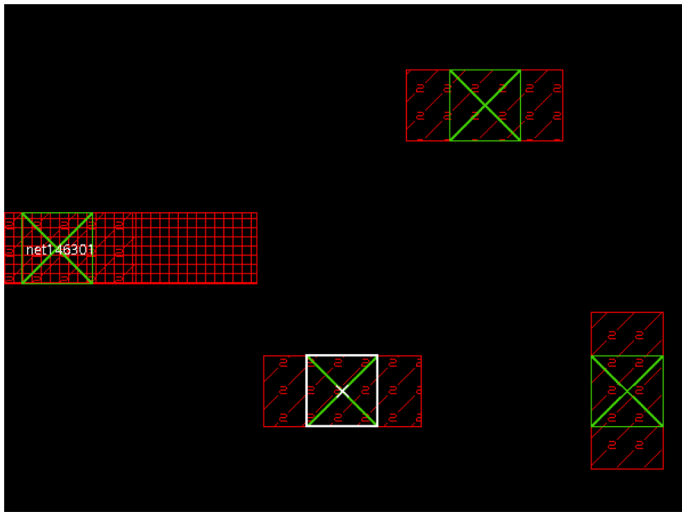
Adjacent cut spacing rule

Dr. CU

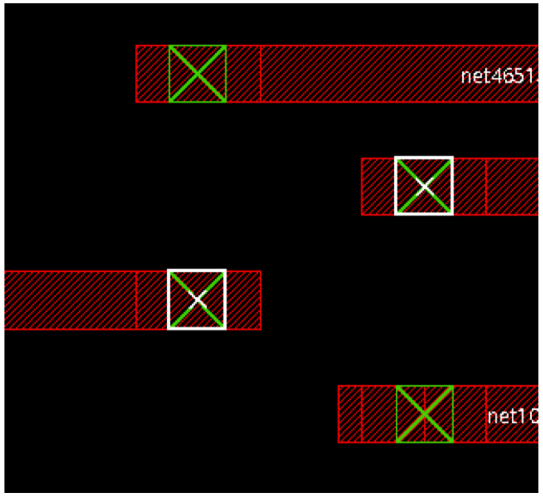



```
LAYER Via2
  TYPE CUT ;
  SPACING 0.075 ;
  WIDTH 0.05 ;
  SPACING 0.155 ADJACENTCUTS 3 WITHIN 0.200 ;
END Via2
```

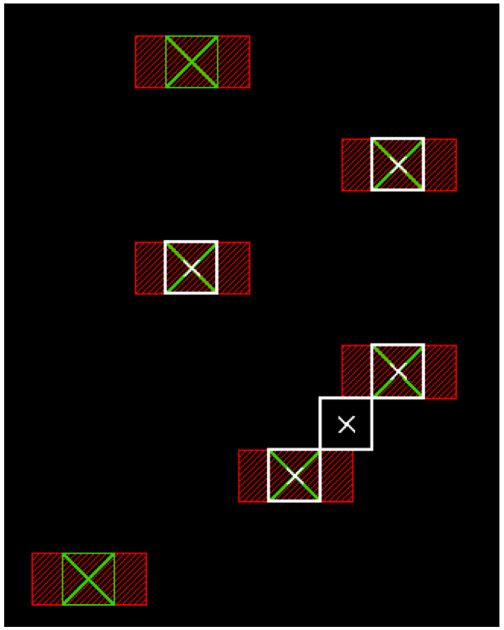
NTUidRoute



Kim & Lee

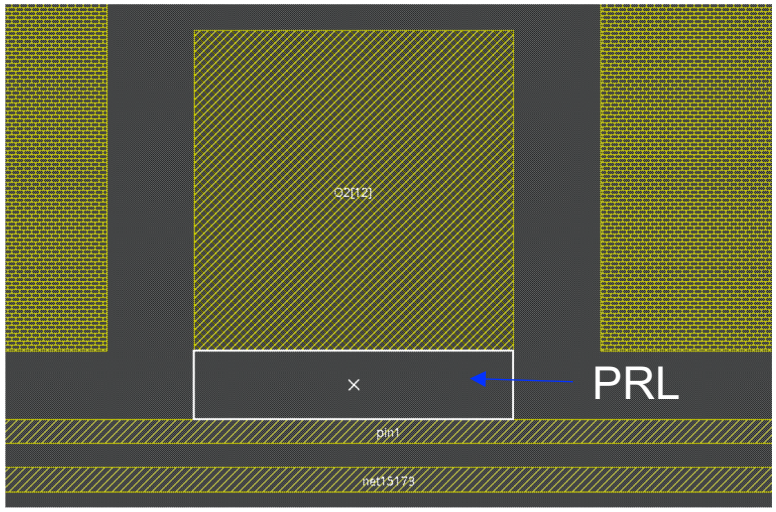


TripleZ

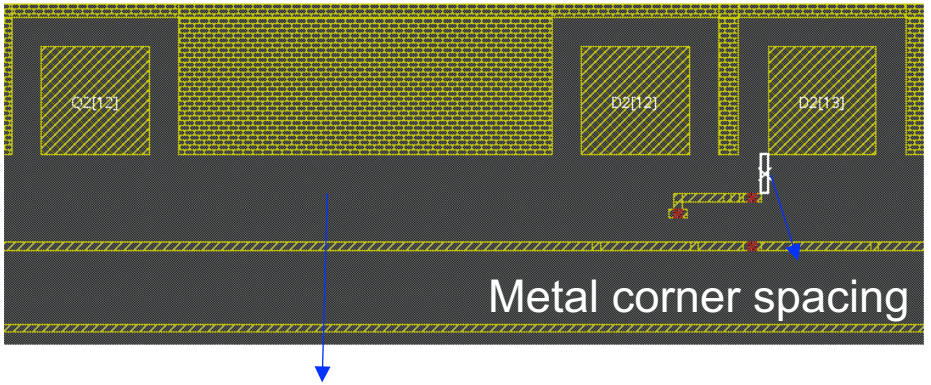


Parallel run length rule

Dr. CU

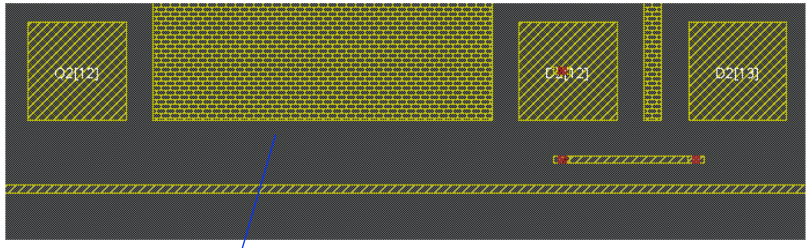


NTUidRoute



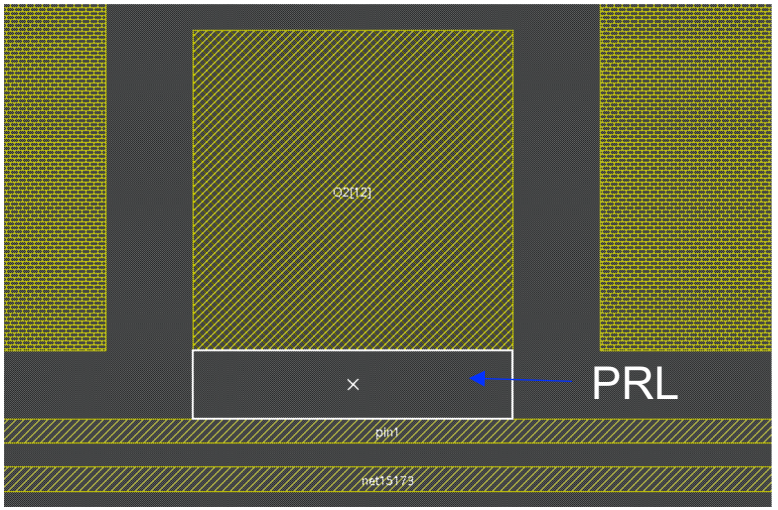
Preventing to route the net close to the shape and avoiding PRL violation

Kim & Lee



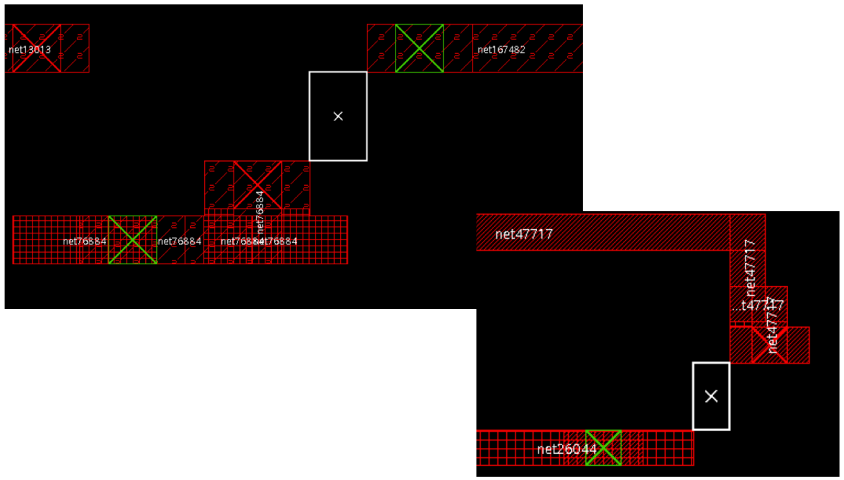
Preventing to route the net close to the shape and avoiding PRL violation. Nice and clean routing over the macro.

TripleZ

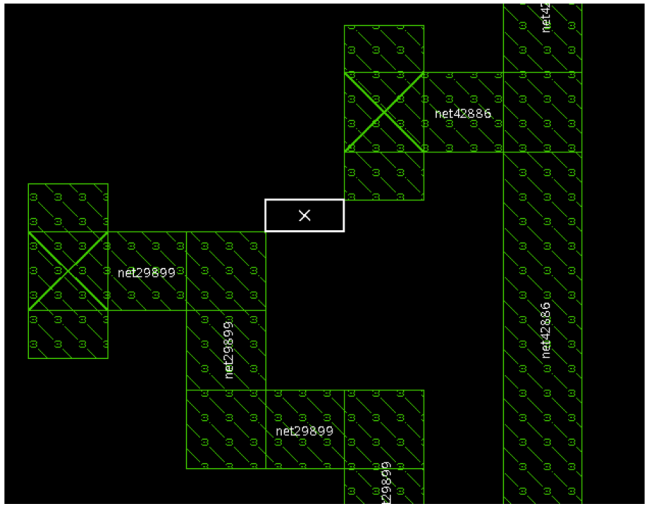


Corner-to-corner spacing rule

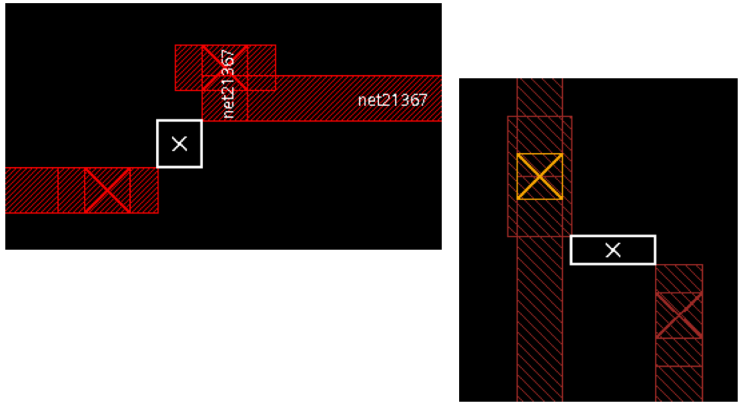
Dr. CU



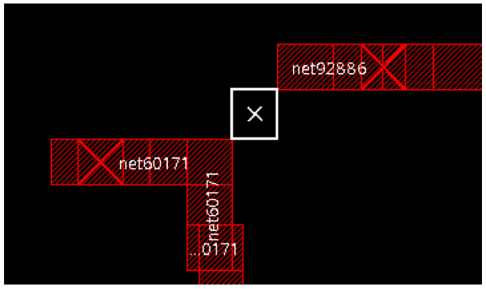
NTUidRoute



Kim & Lee



TripleZ



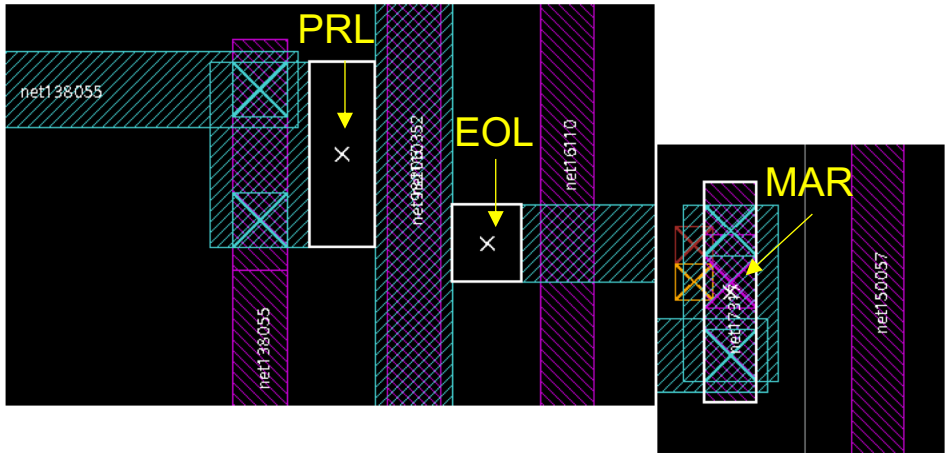
Mainly caused by wrong way routing or bigger via

Double cut via insertion

Dr. CU

No double cut vias been used

NTUidRoute

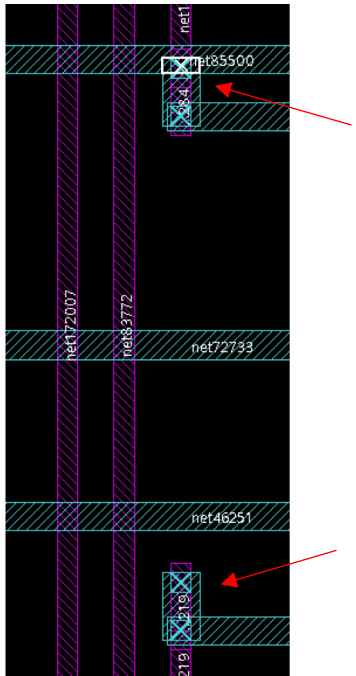


Kim & Lee

No double cut vias been used

When we consider real routing rules, double cut via insertion becomes a very hard problem.
Good research topic.

TripleZ



Challenge is to avoid DRCs when inserting double cut vias

Here it's perfectly inserted

Result Overview

- Memory usage (in GB)

Green : best memory usage with valid solution
Red : out-of-memory
Grey : solution is invalid

	SmartDR	Kim & Lee	TripleZ	NTUidRoute	Dr. CU
test1	27.77	1.72	**0.14**	0.80	1.54
test2	27.70	20.91	**2.58**	5.73	12.30
test3	27.70	2.58	**0.17**	0.82	1.27
test4	27.70	29.29	10.29	**5.15**	12.32
test5		~~0.96~~	~~0.24~~	**1.50**	2.10
test6	27.70	51.52	**6.72**	12.05	10.83
test7		64+	~~13.01~~	24.93	**21.55**
test8		64+	~~24.20~~		**31.41**
test9		64+	~~33.14~~	60.13	**50.53**
test10		64+	~~33.83~~	59.75	**51.65**

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Result Overview

- Usage of Multi-threading
  - CPU time / Real time

Green : highest CPU:Real time ratio

	SmartDR	Kim & Lee	TripleZ	NTUidRoute	Dr. CU
test1	2.18	1.73	0.84	2.24	3.29
test2	1.28	1.65	0.99	4.42	5.90
test3	1.77	1.77	0.87	5.18	4.22
test4	1.03	3.40	0.99	5.44	4.67
test5				5.45	5.64
test6	1.17	1.52	1.00	5.59	6.25
test7				3.70	6.31
test8					6.14
test9				6.82	6.01
test10				6.85	6.07

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DATC RDF

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UFRGS

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https://github.com/rsyn/rsyn-x

Potential Research topics

- Massive parallel detailed routing
- Double cut via insertion
- Nondefault rule (NDR) net handling
- Double/multiple patterning routing