2019 International Symposium on Physical Design

With a Tribute to Professor Alberto Sangiovanni-Vicentelli

San Francisco, California
April 14-17, 2019

Program

The International Symposium on Physical Design provides a high-quality forum for the exchange of ideas on the physical layout design of VLSI, biological or other advanced technology systems. The scope of this symposium includes all aspects of physical design, from high-level interactions with logic synthesis, down to back-end performance optimization and design for manufacturing.
Regular presentations are 30 minutes.

Sunday, April 14

5:30pm - 7:00pm: Reception

Monday, April 15

7:45am - 8:45am: Breakfast

8:45am - 9:00am: General Chair Welcome Message

9:00am - 10:00am: Keynote
Session Chair: Ismail Bustany, Xilinx
"Fusion: The Dawn of the Hyperconvergence Era in EDA", Shankar Krishnamoorthy, Senior Vice President of Digital Implementation at Synopsys (Invited)

10:00am - 10:30am: Morning Break

10:30am - 12:30pm: New Approaches in Placement
Session Chair: Stephen Yang, Xilinx

"How Deep Learning Can Drive Physical Synthesis Towards more Predictable Legalization", Renan Netto, Sheiny Fabre, Tiago Augusto Fontana, Vinicius Livramento, Laercio Pilla, Jose Luis Guntzel; Federal Univ. of Santa Catarina, ASML, Univ. Paris-Sud **(Best Paper Award candidate)**

"Graceful Register Clustering by Effective Mean Shift Algorithm for Balancing Power and Timing", Ya Chu Chang, Tung-Wei Lin, Iris Hui-Ru Jiang, Gi-Joon Nam; National Chiao Tung Univ., National Taiwan Univ., IBM

"Device Layer-Aware Analytical Placement for Analog Circuits", Biying Xu, Shaolan Li, Chak-Wa Pui, Derong Liu, Linxiao Shen, Yibo Lin, Nan Sun, David Pan; Univ. of Texas at Austin, The Chinese Univ. of Hong Kong, Cadence **(Best Paper Award candidate)**

"Analytical Mixed-Cell-Height Legalization Considering Average and Maximum Movement Minimization", Xingquan Li, Jianli Chen, Wenxing Zhu, YaoWen Chang; Univ. Minnan Normal, Univ. Fuzhou, National Taiwan Univ.

12:30pm - 2:00pm: Lunch

2:00pm - 3:30pm: FPGA Special Session: Advances in Adaptable Heterogenenous Computing and Acceleration for Big Data
Session Chair: Mahesh Iyer, Intel

"FPGA-based Computing in the Era of Artificial Intelligence and Big Data", Eriko Nurvitadhi (Intel, invited)

"Advances in Adaptable Computing", Amit Gupta (Xilinx, invited)

"Improving Efficiency and Programmability of Large-Scale Graph Analytics for FPGA Platforms", Mustafa Ozdal (Bilkent University, invited)

3:30pm - 4:00pm: Afternoon break

4:00pm - 6:00pm: Routing in All Forms
Session Chair: Patrick Madden, SUNY Binghamton

"Pin Access-Driven Design Rule Clean and DFM Optimized Routing of Standard Cells under Boolean Constraints", Nikolay Ryzhenko, Steven Burns, Anton Sorokin, Mikhail Talalay; **Intel (Best Paper Award candidate)**

"PSION: Combining Logical Topology and Physical Layout Optimization for Wavelength-Routed ONoCs", Alexandre Truppel, Tsun-Ming Tseng, Davide Bertozzi, Jose Alves, Ulf Schlichtmann; Univ. of Porto, Technical Univ. of Munich, Univ. of Ferrara

"Construction of All Multilayer Monolithic Rectilinear Steiner Minimum Trees on the 3D Hanan Grid for Monolithic 3D IC Routing", Sheng-En David Lin, Dae Hyun Kim; Wash-

ington State Univ.

"RODE: Efficient Routability Diagnosis and Estimation Framework Based on SAT Techniques", Dongwon Park, Ilgweon Kang, Yeseong Kim, Sicun Gao, Bill Lin, Chung-Kuan Cheng; Univ. of California San Diego, Cadence

6:30pm - 9:00pm: Dinner and Social Event

Tuesday, April 16

7:45am - 8:45am: Breakfast

9:00am - 10:00am: Keynote
Session Chair: Noel Menezes, Intel

"A Perspective on Security and Trust Requirements for the Future", Ken Plaks, DARPA program manager of OMG (Obfuscated Manufacturing for GPS) (Invited)

10:00am - 10:30am: Morning Break

10:30am - 12:30pm: Patterning and Machine Learning
Session Chair: Evangeline Young, The Chinese University of Hong Kong

"Declarative Language for Geometric Pattern Matching in VLSI Process Rule Modeling", Gyuszi Suto, Geoff Greenleaf, Sanjay Soni, Heinrich Fischer, Phanindra Bhagavatula, Renato Hentschke, Brian Miller; Intel

"Electromigration-Aware Interconnect Design", Sachin S. Sapatnekar (University of Minnesota, invited)

"Toward Intelligent Physical Design: Deep Learning and GPU Acceleration", Haoxing Ren (Nvidia, invited)

"Multiple Patterning Layout Compliance with Minimizing Topology Disturbance and Polygon Displacement", Hua-Yu Chang, Iris Hui-Ru Jiang; Synopsys, National Taiwan Univ.

12:30pm - 2:00pm: Lunch

2:00pm - 3:30pm: Cyber Physical Systems Session
Session Chair: Patrick Groeneveld, Cadence Design Systems

"From Electronic Design Automation to Automotive Design Automation", Chung-Wei Lin (National Taiwan University, invited)

"Enterprise-wide AI-enabled Digital Transformation", Mehdi Maasoumy (University of California at Berkeley, invited)

"Secure and Trustworthy Cyber-Physical System Design: A Cross-Layer Perspective", Pierluigi Nuzzo (USC, invited)

3:30pm - 4:00pm: Afternoon break

4:00pm - 6:00pm: Tribute to Professor Alberto Sangiovanni Vicentelli
Session Chair: Pierluigi Nuzzo, University of Southern California

"The Slow Start of Fast Spice: a Brief History of Timing", Jacob White (MIT, invited)

"Basic and Advanced Researches in Logic Synthesis and their Industrial Contributions", Masahiro Fujita (University of Tokyo, invited)

"From Electronic Design Automation to Cyber-Physical System Design Automation: A Tale of Platform-Based Design", Pierluigi Nuzzo (USC, invited)

"My 50-Year Journey from Punched Cards to Swarm Systems", Alberto Sangiovanni-Vincentelli (University of California at Berkeley, invited)

6:30pm - 9:00pm: Lifetime Achievement Award Dinner Banquet

Wednesday, April 17

7:45am - 8:45am: Breakfast

8:45am - 10:15am: Physical Design - Where are we going?
Session Chair: C.K. Cheng, University of California at San Diego

"Analog Layout Synthesis: Are we there yet?", Prasanth Mangalagiri (Intel, invited)

"Lagrangian Relaxation Based Gate Sizing With Clock Skew Scheduling - A Fast and Effective Approach", Ankur Sharma, David Chinnery, Chris Chu; Mentor Graphics Corporation, Univ. Iowa State

"Adaptive Clustering and Sampling for High-Dimensional and Multi-Failure-Region SRAM Yield Analysis", Xiao Shi, Hao Yan, Jinxin Wang, Xiaofen Xu, Fengyuan Liu, Longxing Shi, Lei He; Univ. of California Los Angeles, Univ. Southeast

10:15am - 10:30pm: Morning Break

10:30am - 12:00pm: Routing Contest
Session Chair: David Chinnery, Mentor Graphics

"ISPD 2019 Initial Detailed Routing Contest and Benchmarks with Advanced Routing Rules", Gracieli Posser

12:00pm - 1:00pm: Lunch

1:00pm - 1:45pm: Poster Session

2:00pm - 3:30pm: Special Panel on ML in Physical Design: Opportunities, Infrastructure, and Deployment.
Session Chair: Ismail Bustany Xilinx

Panelists: Ivan Kissiov, Mentor Graphics; Harold Levy, Synopsys; Ashish Sirasao, Xilinx; Haoxing Ren, Nvidia; Laleh Behjat, University of Calgary

4:00pm - 6:00pm: Social Event