

2010 International Symposium on Physical Design

Marriott Fisherman's Wharf, San Francisco, California

March 14-17, 2010

www.ispd.cc

Sponsored by ACM/SIGDA with Technical Co-Sponsorship from IEEE CAS
Additional support from Cadence, IBM Research, Intel Corporation, Mentor Graphics,
SpringSoft, Sun Microsystems, and Synopsys

PROGRAM

The International Symposium on Physical Design provides a high-quality forum for the exchange of ideas on the physical layout design of VLSI and biological systems. The scope of this symposium includes all aspects of physical design, from high-level interactions with logic synthesis, down to back-end performance optimization and design for manufacturing.

Each regular paper presentation runs 25 minutes. Each invited talk is 30 minutes.

SUNDAY, March 14

5:30 – 7:00 pm: Evening Reception

MONDAY, March 15

8:30 – 9:40 am: Welcome and Keynote Address

Host: Prashant Saxena (*Synopsys*)

(Keynote Talk) Physical Design of Biological Systems

Louis K. Scheffer from Howard Hughes Medical Institute

9:40 – 10:10 am: Morning Break

10:10 am - 12:10 pm Session 1: Modern Physical Design Challenges

Chair: Lars Hagen (*Cadence*)

(Invited talk) Going with the Flow: Bridging the Gap between Theory and Practice in Physical Design

Patrick Groeneveld from Magma

(Invited talk) Design Planning Trends and Challenges

Neeraj Kaul from Synopsys

(Invited talk) Physical Design Challenges beyond the 22nm Node

Sani Nassif and Kevin Nowka from IBM

(Invited talk) Challenges and Opportunities in Optimization of Automotive Electronics

Serge Leef from Mentor Graphics

12:10 – 2:00 pm: Lunch

2:00 – 4:15 pm Session 2: Advances in Routing

Chair: Mustafa Ozdal (*Intel*)

(Invited talk) What Makes a Design Difficult to Route

Charles Alpert, Zhuo Li, Michael Moffitt, Gi-Joon Nam, Jarrod Roy, and Gustavo Tellez from IBM

FOARS: FLUTE Based Obstacle-Avoiding Rectilinear Steiner Tree Construction

Gaurav Ajwani, Chris Chu and Wai-Kei Mak

Completing High-Quality Global Routes

Jin Hu, Jarrod Roy and Igor Markov

(Invited talk) Thinking Outside of the Chip

John Park from Mentor Graphics

B-Escape: A Simultaneous Escape Routing Algorithm Based on Boundary Routing

Lijuan Luo, Tan Yan, Qiang Ma, Martin Wong and Toshiyuki Shibuya

4:15 – 4:45 pm: Afternoon Break

4:45 – 6:10 pm Session 3: Analog Design Automation

Chair: Lei He (*UCLA*)

(Invited talk) Analog Layout Synthesis: What's Missing?

Rob Rutenbar from University of Illinois

(Invited talk) Design Platform for Electrical and Physical Co-Design of Analog Circuits

Mar Hershenson from Magma

Automatic Generation of Hierarchical Placement Rules for Analog Integrated Circuits

Michael Eick, Martin Strasser, Helmut Graeb and Ulf Schlichtmann

6:10 – 9:00 pm: Dinner Banquet

TUESDAY, March 16

8:30 – 10:25 am Session 4: Physical Design for 3D ICs

Chair: Sung Kyu Lim (*Georgia Institute of Technology*)

(Invited talk) Adding a New Dimension to Physical Design

Sachin Sapatnekar from University of Minnesota

(Invited talk) Physical Design Implementation for 3D IC: Methodology and Tools

Dave Noice from Cadence

(Invited talk) Efficient Design Practices for Thermal Management of a TSV Based 3D IC System
Zongwu Tang from Synopsys

An Analytical Placer for Mixed-Size 3D Placement
Jason Cong and Guojie Luo

10:25 – 10:55 am: Morning Break

10:55 am – 12:35 pm Session 5: Physical Synthesis
Chair: Igor Markov (*University of Michigan*)

Logical and Physical Restructuring of Fan-In Trees
Hua Xiang, Haoxing Ren, Louise Trevillyan, Lakshmi Reddy, Ruchir Puri and Minsik Cho.

Ultra-Fast Interconnect Driven Cell Cloning for Minimizing Critical Path Delay
Zhuo Li, David Papa, Charles Alpert, Shiyang Hu, Weiping Shi, Cliff Sze and Ying Zhou

ITOP: Integrating Timing Optimization within Placement
Natarajan Viswanathan, Gi-Joon Nam, Jarrod Roy, Zhuo Li, Charles Alpert, Shyam Ramji and Chris Chu.

Physical Synthesis of Bus Matrix for High Bandwidth Low Power On-Chip Communications
Renshen Wang, Evangeline Young, Ronald Graham and Chung-Kuan Cheng

12:35 – 2:00 pm: Lunch

2:00 – 3:40 pm Session 6: Design for Manufacturing
Chair: Ting-Chi Wang (*National Tsing-Hua University*)

Dummy Fill Optimization for Enhanced Manufacturability
Yaoguang Wei and Sachin Sapatnekar

Density Gradient Minimization with Coupling-Constrained Dummy Fill for CMP Control
Huang-Yu Chen, Szu-Jui Chou and Yao-Wen Chang

Total Sensitivity Based DFM Optimization of Standard Library Cells
Yongchan Ban, Savithri Sundareswaran and David Z. Pan

A Matching Based Decomposer for Double Patterning Lithography
Yue Xu and Chris Chu

3:40 – 4:10 pm: Afternoon Break

4:10 – 5:40 pm Session 7: Advances in Clock Tree Designs and ISPD'10 Clock Tree Synthesis Contest

Chair: Cliff Sze (*IBM Research*)

Skew Management of NBTI Impacted Gated Clock Trees
Ashutosh Chakraborty and David Z. Pan

Accurate Clock Mesh Sizing via Sequential Quadratic Programming
Venkata Rajesh Mekala, Yifang Liu, Xiaoji Ye, Jiang Hu and Peng Li

(Invited talk) ISPD 2010 High Performance Clock Network Synthesis Contest: Benchmark Suite and Results
Cliff Sze from IBM Research

6:00 – 9:00 pm: Dinner Banquet

WEDNESDAY, March 17

8:30 – 10:40 am Session 8: Performance and Reliability Optimization

Chair: Linda Huaizhi Wu (*Synopsys*)

(Invited talk) Impact of Local Interconnects on Timing and Power in a High Performance Microprocessor
Rupesh Shelar and Marek Patyra from Intel

Interconnect Power and Delay Optimization by Dynamic Programming in Gridded Design Rules
Konstantin Moiseev, Avinoam Kolodny and Shmuel Wimer

Performance Study of VeSFET-Based, High-Density Regular Circuits
Yi-Wei Lin, Malgorzata Marek-Sadowska and Wojciech Maly

A Statistical Framework for Designing On-Chip Thermal Sensing Infrastructure in Nano-Scale Systems
Yufu Zhang, Bing Shi and Ankur Srivastava

Optimal Wiring Topology for Electromigration Avoidance Considering Multiple Layers and Obstacles
Iris Hui-Ru Jiang, Hua-Yu Chang and Chih-Long Chang

10:40 – 11:10 am: Morning Break

11:10 am – 12:25 pm Session 9: Clustering and Biochip Placement & Routing

Chair: Jens Lienig (*Dresden University of Technology*)

SafeChoice: A Novel Clustering Algorithm for Wirelength-Driven Placement
Jackey Z. Yan, Chris Chu and Wai-Kei Mak

Droplet-Routing-Aware Module Placement for Cross-Referencing Biochips
Zigang Xiao and Evangeline F. Y. Young

A Two-Stage ILP-Based Droplet Routing Algorithm for Pin-Constrained Digital Microfluidic Biochips
Tsung-Wei Huang and Tsung-Yi Ho

12:25 – 12:40 pm: Closing Remarks

12:40 – 2:00 pm: Lunch

SYMPOSIUM REGISTRATION

Please register on-line at <http://www.ispd.cc> by **February 17th, 2010 (Wednesday)** for the early registration discount rates.

Registration Rates	Early	Late
ACM/IEEE Member	\$380	\$455
Non-Member	\$455	\$530
Student	\$180	\$235

HOTEL ACCOMODATIONS AND TRAVEL

The 2010 ISPD will be held at the Marriott Fisherman's Wharf, San Francisco, California. It will be co-located with the ACM International Workshop on Timing Issues in the Specification and Synthesis of

Digital Systems (TAU Workshop). The workshop will be held on March 18 - 19, 2010.

Marriott Fisherman's Wharf, San Francisco, California
1250 Columbus Avenue San Francisco, CA 94133, US
Room Rate: \$129 (complimentary internet access in guestrooms)

Reservations to be made no later than **February 12, 2010** for this discounted rate. You can visit <http://www.marriott.com/> and book your reservation by providing the group code of **ACMACMA** to the group code box. You may also call 1-800-525-0956 (toll-free in the U.S.) or 1-415-775-7555. Be sure to identify yourself as a member of ACM conference attendees for ISPD.

Symposium Organization

General Chair

Prashant Saxena / *Synopsys*

Past Chair

Gi-Joon Nam / *IBM Research*

Steering Committee

Patrick Groeneveld / *Magma*, Shankar Krishnamoorthy (*Mentor Graphics*),
Malgorzata Marek-Sadowska (*UCSB*), Gi-Joon Nam / *IBM Research* (Chair),
David Z. Pan (*University of Texas at Austin*)

Technical Program Chair

Yao-Wen Chang / *National Taiman University*

Technical Program Committee

Ameya Agnihotri / *Magma*

Yao-Wen Chang / *NTU*

Hongyu Chen / *Mentor Graphics*

C.-K. Cheng / *UCSD*

Yi-Kan Cheng / *TSMC*

Salim Chowdhury / *Sun*

Helmut Graeb / *Tech. U Muenchen*

Lars Hagen / *Cadence*

Masanori Hashimoto / *Osaka U*

Lei He / *UCLA*

Jiang Hu / *Texas A&M U*

Andrew Kennings / *U of Waterloo*

Cheng-Kok Koh / *Purdue U*

Igor Markov / *U of Michigan*

Seungweon Paek / *Samsung*

Rupesh Shelar / *Intel*

Ankur Srivastava / *U. of Maryland*

Cliff Sze / *IBM Research*

Ting-Chi Wang / *National Tsing Hua U*

Martin D. F. Wong / *UIUC*

Linda Huaizhi Wu / *Synopsys*

Evangeline Young / *Chinese U of Hong Kong*

Yaping Zhan / *AMD*

Publication Chair

Jiang Hu (*Texas A&M University*)

Publicity Chair/Webmaster

Cheng-Kok Koh (*Purdue University*)

Contest Chair

Cliff Sze (*IBM Research*)