DATC Robust Design Flow

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March 21, 2021

GitHub Link: https://github.com/ieee-ceda-datc
Design Automation Technical Committee (DATC)

- **A technical committee of IEEE CEDA**
  - Provide a forum for discussing strategies and issues in design automation

- **Task: DATC Robust Design Flow (RDF)**
  - Academic reference **RTL-to-GDS** design flow
  - **Free** for academic and noncommercial research
  - A complete RTL-to-GDS paths for *any* use also available

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<tr>
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<th>Affiliation</th>
<th>Role</th>
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DATC Robust Design Flow (RDF)

- **Academic reference design flow**
  - Initiated 2016; last updated 2020
  - Synthesis to detailed routing flow built upon outstanding contest-winning academic tools
  - Also supports complete RTL-to-GDS flow with OpenROAD tool chains

- **RDF Goal:**
  1. Preserve and integrate leading research codes, including contest outcomes
  2. Trigger design flow and cross-stage optimization research via various EDA tools developed from academia

- **GitHub repository**
  [https://github.com/ieee-ceda-datc/datc-robust-design-flow](https://github.com/ieee-ceda-datc/datc-robust-design-flow)
New Direction: Calibrations

- **Goal**: support academic research on analyses and verifications
- Start with **DRV-free** routed testcases in open enablements
  - \{NanGate45, SKY130, ASAP7\} × \{AES, JPEG, IBEX, SWERV\}
    - Routed *.v, *.def, *.sdc, and *.spef
- Provides **calibration data for STA, RCX, and IR drop analysis in JSON**

Visualized calibration designs from OpenROAD-GUI
Calibrations: RCX and STA

- **RCX**: via `.spef` files directly
- **STA**: `endpoint_slacks.json`
  - Setup slack values at every flip-flop D pin
- **STA**: `5_worst.json`
  - Block-level WNS, TNS, and failing paths
  - Detailed report of top 5 worst timing paths

```
"tech": "freepdk45",
"design": "aes_cipher_top",
"pins": [
  "28572_/D",
  "28573_/D",
  ...
],
"slacks": [
  "0.648",
  "0.731",
  ...
]

"top1": {
  "endPoint": "28884_/D",
  "endPointStatus": "Rising",
  "startPoint": "28827_/Q",
  "startPointStatus": "Falling",
  ...
  "slack": "-0.230",
  "pathList": [
    {
      "pin": "clk",
      "status": "Rising",
      "net": "clk",
    }
  ]
}
```

Example of NanGate45 AES Timing Report from 5-worst JSON

```
aes_cipher_top (freepdk45) (freepdk45) Summary
========================================================

WNS: -0.230
TNS: -10.560
FEP: 139

---------------------------------------------------------
aes_cipher_top (freepdk45) top1 worst timing path
---------------------------------------------------------
Startpoint: _28827_/Q (Falling)
Endpoint: _28884_/D (Rising)
Path Group: reg2reg

Delay  Time  Description
--------  --------  ---------------
0.00 0.00 ^ clk
0.01 0.01 ^ clkbuf_0_clk/A (BUF_X4)
0.03 0.04 ^ clkbuf_0_clk/Z (BUF_X4)
...  
0.00 1.23 ^ clkbuf_4_6_0_clk/A (CLKBUF_X1)
0.08 1.31 ^ clkbuf_4_6_0_clk/Z (CLKBUF_X1)
0.00 1.32 ^ clkbuf_6_27_f_fclk/A (BUF_X4)
0.03 1.35 ^ clkbuf_6_27_f_fclk/Z (BUF_X4)
0.00 1.35 _28884_/CK (DFF_X1)
0.04 1.31 library setup time
 1.31 data required time
 1.54 data arrival time

-0.23 slack (VIOLATED)
```

Endpoint slacks JSON
5-worst JSON

https://github.com/ieee-ceda-datc/datc-rdf-timer-calibration
Calibrations: IR Drop Analysis

- Two JSON formats:
  - (1) **Voltage source** and (2) **instance voltage**

```json
vsr.c.json
{
  "summary": {
    "design": design_name,
    "numVddSrcs": 1,
    "numVssSrcs": 1,
    "tech": "sky130",
    "vdd": 1.8,
    "voltageSrcMetalLayer": "met4",
    "vss": 0
  }
  "detail": {
    "voltageSrcList": [{
      "type": "VDD",
      "voltageSrcName": "VDD100",
      "xLocation": 12.0,
      "yLocation": 12.0
    },
    {
      "type": "VSS",
      "voltageSrcName": "VSS101",
      "xLocation": 544.0,
      "yLocation": 12.0
    }]
  }
}
```

```json
instance_voltage.json
{
  "summary": {
    "design": design_name,
    "powerNet": net_name,
    "tech": ,
    "timingCorner": "tt_02SC_1v80",
    "vdd": 1.8000,
    "vss": 0,
    "wir": {
      "instanceName": "_28766_",
      "ir": 0.0310,
      "layer": "met1",
      "voltage": 1.7690
    }
  }
  "detail": {
    "instanceList": [
      "_28766_", "FILLER_170_1364",
      "FILLER_170_1362"
    ],
    "voltages": [1.7690, 1.7690, 1.7691]
  }
}
```
Summary

- **DATC Robust Design Flow (RDF)**
  - Provides RTL-to-GDS flow with leading research codes, including from past academic contests and from recent OpenROAD tools
  - Shed light on flow-scale/cross-stage optimization research via various EDA tools developed from academia

- **New direction: Calibration**
  - Provides calibration data to support academic research on analyses and verifications
  - Started with STA, RCX, and IR drop analysis
  - **Coming soon**: Metrics dataset being compiled for supporting ML-CAD research

- **We are open!** Please give any suggestion and contribute to our effort!

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