Tutorial on Design For Manufacturability for Physical Design

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Overview of Presentation

- Yield Loss Mechanism Evolution
- Classification of DFM Approaches
- True DFM: Defining Proactive DFM
- Necessary Conditions for Proactive DFM
- Process Characterization
- Design Flows that Provide Proactive DFM
- DFM Results
- Looking into the Future: Extreme Layout Regularity
Random defects are no longer the dominant yield loss mechanism.
- Yields are limited by design features, systematic and parametric effects.
## Random Yield Loss Mechanisms – Al Interconnect

<table>
<thead>
<tr>
<th>Type</th>
<th>Yield Loss Mechanisms</th>
</tr>
</thead>
<tbody>
<tr>
<td>Random</td>
<td>Active, poly and metal shorts and opens due to particle defects</td>
</tr>
<tr>
<td></td>
<td>Contact and via opens due to formation defectivity</td>
</tr>
</tbody>
</table>
Systematic Yield Loss Mechanisms - Cu Interconnect

- Misalignment, line-ends/borders
- Contact/via opens due to local neighborhood effects (e.g. pitch/hole size)
- Leakage from STI related stress
- Impact of micro/macro loading design rule marginalities
- Misalignment, line-ends/borders

**Chart:**
- **Y-AXIS:** Via Failure Rate (fpb)
- **X-AXIS:** Pitch (um)
- Graph shows an increase in failure rate with decreasing pitch.
**Systematic Yield Loss: Printability – Nanometer Era**

<table>
<thead>
<tr>
<th>Type</th>
<th>Yield Loss Mechanisms</th>
</tr>
</thead>
<tbody>
<tr>
<td>Systematic</td>
<td>Poor contact coverage due to misalignment and defocus/pull back</td>
</tr>
<tr>
<td>Poly/Metal shorts</td>
<td></td>
</tr>
<tr>
<td>Material opens</td>
<td></td>
</tr>
</tbody>
</table>
Parametric Yield Loss Mechanisms – Nanometer Era

Environment dependent poly CD variation

ACLV / CD Variation

<table>
<thead>
<tr>
<th>Type</th>
<th>Yield Loss Mechanisms</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parametric</td>
<td>Performance variation from lithography effects</td>
</tr>
<tr>
<td></td>
<td>e.g., contact/via coverage, active/poly flaring, CD variation</td>
</tr>
<tr>
<td>Dummy fill parasitic effects</td>
<td></td>
</tr>
<tr>
<td>Device mismatch</td>
<td></td>
</tr>
<tr>
<td>Non-physical corner modeling</td>
<td></td>
</tr>
</tbody>
</table>
Technology Challenges: Implications for Manufacturability

90nm
- Back-end integration issues
- Low k: stress and reliability
- CMP - multi-layer topography issues
- Product ramp issues
- Variability
- Yield-performance tradeoffs

65nm
- Litho:
  - OPC/PSM integration issues w/photo window (DOF)
- Front-end/Transistor
  - Layout dependent performance
- Product ramp issues
  - Parametric variations - > yield loss

45nm
- Litho:
  - Layout pattern dependence, Scanner NA, Immersion litho, OPC/PSM integration, issues w/photo window (DOF)
- Front end/Transistor
  - New transistor architectures (UTB, DG SOI)
- Product ramp issues
  - Reliability assurance
DFM is a Business Opportunity
"Seamless" DFM Can Contribute 5% More Good Die

What's 5% more good die worth?

- $50M over the life of a cell phone
- $80M over the life of a game chip
- $100M per year per fab at 90nm
A Brief History of DFM

Functional Yield means Rules

- Design rules guarantee yield!...well, not really...
- ...then recommended rules
- ...and opportunistic design data base post-processing to enforce them

Performance Yield is Covered by Corners

- The corners represent the process
- ...The corners don’t represent the process but they are conservative
- ...Within chip variations are important so..
  - Restrict transistor layouts?
  - Statistical timing simulation?

Idsat Distribution

ASIC Corners

Realistic Corners
**Proactive DFM**

- DFM needs to be Proactive
- Occurring early in the design flow
- Up-front accurate process characterization
- Yield modeling to characterize IP and drive EDA tools

- Designer access to the process is limited
- Most DFM today is Reactive
  - Increase in design cycle time
  - Misaligned mask GDSII and design database
  - Risky design feature changes

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**Design**
- IP lib. Design
- Physical SP&R

**Verification and Yield Opt.**
- Timing and SI Analyses
- Post-GDS Yield Opt.
- Dummy Fill and Cheesing

**Manufacturing**
- MDP and Mask Making
- Yield Ramp

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**Process Characterization + Yield Modeling**
Necessary Conditions for Pro-Active DFM

- Accurate characterization of design-interactions at target fab(s)
- Effects modeled across the whole process window
- Quantification of alternatives that allow EDA tools to make millions of DFM trade-offs
- Integration early in the design flow where there are more degrees of freedom
  - Floor planning
  - SP&R
- Modifications made prior to verification
Yield Simulation is Core to Proactive DFM

Yield Simulation allows for better understanding of the DFM universe

- A yield model for DFM:
  - Model of failure rate of a design element (e.g., transistor, contact, via) as a function of the layout design
  - Example:
    - What is the failure rate of a single via vs. double?
    - What is the probability of a short in two metal lines if there are lots of vias underneath them

- To do this, we need process characterization
Yield Loss Mechanisms

- Layer defect densities
- Attribute dependent failure rates
- Lithography / CMP driven interactions
- ...

**Yield Loss Mechanisms (YLM’s)**

- Root causes of process related yield loss
- Each YLM must be characterized in the process with a specific test structure – Characterization Vehicle (CV)
Typical Die Yield Estimation

Model implies that for a given die size, yield is based only upon process maturity – this is not correct

- Yield is different for different IP content
- Process defectivity is different for each module

\[ Y = e^{-D_0A} \]

where,

\[ Y = \text{die yield} \]

\[ D_0 = \text{mean defects (1/cm}^2 \text{)} \]

\[ A = \text{die area (cm}^2 \text{)} \]
Chip Yield is a strong function of design content

- Physical design features interact with specific module weakness
Accurate Process Characterization

**Defect Size Distribution by Process Module**

- **Metal Opens/Shorts Characterization Vehicle**
- **Poly and Active Opens/Shorts Characterization Vehicle**

\[ DSD(x) = \text{defect size/count distribution} \]
Product Design Attributes

<table>
<thead>
<tr>
<th>I/O</th>
<th>SRAM</th>
<th>ROM</th>
<th>Custom Logic</th>
<th>Analog</th>
</tr>
</thead>
</table>

**Design Attributes**
- Widths, lengths and spacing
- Counts
- Densities
- Overlaps/enclosures
- ...

- **Design Attributes:**
  - Physical design properties that interact with specific module marginalities
  - Each attribute can be extracted from physical layout
  - Design attribute extraction (DAE) enables quantification of design content specific YLM models
Design Attribute Extraction

Contacts/Via Counts
- N/P Active
- Poly
- V1-Vx

Critical Area Shorts
- AA
- Poly
- M1-Mx

Contact/Via Count Design Attribute Extraction

\[ A_C(x) = \text{design attribute sensitivity to } x \]
Accurate Process Characterization

DOE on litho parameters
RSM of layout metric

INPUT: Characterization of litho process statistics

Yield, Performance, Profitability
Implicit YLM model: process window effects

Process Margin data from CV

PSD: condition 1

PSD: condition 2
**Yield Simulation Results: Yield Impact Matrix**

**Design Attributes**
- Widths, lengths and spacing
- Counts
- Densities
- Overlaps/enclosures
- ...

- Physical design properties that interact with specific module defectivities
- Each attribute can be extracted from GDSII
- Design attribute extraction (DAE) enables quantification of die content specific yield models

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<table>
<thead>
<tr>
<th>Random Defects</th>
<th>Failure Mode</th>
<th>Full Chip</th>
<th>SRAM</th>
<th>LOGIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active</td>
<td>Random</td>
<td>98%</td>
<td>99%</td>
<td>99%</td>
</tr>
<tr>
<td></td>
<td>Pattern Dependent Total</td>
<td>97%</td>
<td>98%</td>
<td>99%</td>
</tr>
<tr>
<td>Poly</td>
<td>Random</td>
<td>97%</td>
<td>98%</td>
<td>99%</td>
</tr>
<tr>
<td></td>
<td>Pattern Dependent Total</td>
<td>94%</td>
<td>95%</td>
<td>99%</td>
</tr>
<tr>
<td>Metal</td>
<td>Random</td>
<td>97%</td>
<td>98%</td>
<td>99%</td>
</tr>
<tr>
<td></td>
<td>Pattern Dependent Total</td>
<td>94%</td>
<td>95%</td>
<td>99%</td>
</tr>
<tr>
<td>Holes</td>
<td></td>
<td>97%</td>
<td>98%</td>
<td>99%</td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td>81%</td>
<td>82%</td>
<td>99%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Systematic</th>
<th>Failure Mode</th>
<th>Full Chip</th>
<th>SRAM</th>
<th>LOGIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal Islands</td>
<td></td>
<td>87%</td>
<td>89%</td>
<td>90%</td>
</tr>
<tr>
<td>Pattern Density</td>
<td></td>
<td>91%</td>
<td>93%</td>
<td>94%</td>
</tr>
<tr>
<td>Narrow Space Wide Neighbor</td>
<td></td>
<td>97%</td>
<td>99%</td>
<td>100%</td>
</tr>
<tr>
<td>Via induced Metal Shorts</td>
<td></td>
<td>77%</td>
<td>78%</td>
<td>79%</td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td>62%</td>
<td>64%</td>
<td>64%</td>
</tr>
</tbody>
</table>
Yield modeling accuracy is excellent when you characterize right

- Error represents unidentified yield loss mechanisms or lack of yield model
Overview of Layout Design for Manufacturability

- **Critical Area Based Wire Spreading**
  - Most useful in Al interconnect era (random metal shorts – dominant yield loss mechanism)

- **Contact/via Doubling**
  - Effective in reduction yield losses due to random hole opens (Al & Cu)

- **Systematic Yield Model Based Local and Global P&R Layout Modifications**
  - Essential for 3-D topography effects due to Cu CMP and low-k interconnect

- **Printability and Performance Variability Driven Layout Generation**
  - Absolute must in the Nanometer Era
  - Pro-active (not afterthought in RET)
Limited Yield Optimization

Product yields must be optimized by improving LY’s
- $LY_{GAIN}$ → ratio of improvement for any specific optimization

Prioritizing which LY’s to improve requires an understanding of the specific **Design Manufacturability Objectives**
Design Manufacturability Objectives

- **Customization of DFM objectives**
  - High volume parts in mature process
  - Lower volume parts during ramp

<table>
<thead>
<tr>
<th>Objectives</th>
<th>Products</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average Yield</td>
<td>DVD, STB, Cell Phone, Digital Cameras</td>
</tr>
<tr>
<td>Yield Variability</td>
<td>Networking, Graphics, DSP</td>
</tr>
<tr>
<td>Performance Variability</td>
<td>Microprocessors</td>
</tr>
<tr>
<td>Custom</td>
<td>Tailored specifically for a process and product</td>
</tr>
</tbody>
</table>
Enabling Proactive DFM For Designers

Three components to enable Proactive DFM
- DFM library module
- Layout attribute dependent yield models (DFM library view)
- Yield simulation and optimization software
DFM Variant Generation Flow

DFM Architecture Specifications

- Average Yield
- Yield Variability
- Performance Variability

Netlist → Layout Design

Cell Layouts

Manufacturability Hot Spot Localization

Constraint generation

Hot Spots Minimized? Yes → DFM Library

No → MFG Characterization

Pruning

Yield, Performance, Profitability
Yield Variants Example

High Density

Random/Systematic Yield Variant

Litho hot spots

M1 shorts

M1 opens

Yield/Speed Consistency Variant

+20% area
-50% FR (ppb)

+40% area
-50% FR (ppb)
-85% YV (std.dev)

Yield, Performance, Profitability
Standard Cell Optimization Flow

**Original Netlist**

- MOS1 d g s b nmos L=0.13u W=1u
- MOS2 d g s b pmos L=0.13u W=0.8u
- MOS3 d g s b nmos L=0.13u W=0.7u
- MOS4 d g s b pmos L=0.13u W=1.2u
- MOS5 d g s b nmos L=0.13u W=1.3u
- MOS6 d g s b pmos L=0.13u W=1u

**Cell Architecture**

- Contact redundancy definition
- Spacing rules definition
- Transitions rules definition
- Metal islands definition
- Taps
  ...

**Synthesized Layout**

**Litho Environment**

**Litho Simulated Layout**

**Hot Spot Analysis**

**Optimized Layout**

MOS1 d g s b nmos L=0.13u W=1u
MOS2 d g s b pmos L=0.13u W=0.8u
MOS3 d g s b nmos L=0.13u W=0.7u
MOS4 d g s b pmos L=0.13u W=1.2u
MOS5 d g s b nmos L=0.13u W=1.3u
MOS6 d g s b pmos L=0.13u W=1u
DFM Library View for EDA

- .pdfm view includes relevant data to enable EDA tools to make yield tradeoffs:
  - Process Defectivities
  - Design Attributes
  - Yield and Manufacturability Models

- .pdfm data also enables BEOL routing optimization

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Library View</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layout</td>
<td>GDSII</td>
</tr>
<tr>
<td>Schematic</td>
<td>SPICE Netlist</td>
</tr>
<tr>
<td>P&amp;R Footprint</td>
<td>LEF</td>
</tr>
<tr>
<td>Performance</td>
<td>.lib</td>
</tr>
<tr>
<td>Logic Function</td>
<td>Verilog</td>
</tr>
<tr>
<td>Manufacturability</td>
<td>.pdfm</td>
</tr>
</tbody>
</table>
“pDfx enabled” P&R

- Include yield in the cost function
- Take advantage of design slacks
- Timing convergence properties unchanged
Silicon shows up to 12% GDPW improvement by applying our Proactive DFM methodology
Looking Into the Future: Extreme Layout Regularity

- RETs are time-consuming and difficult to optimize for large process windows
  - Defocus, Illumination conditions, Pattern neighborhood

- Conventional design rules are becoming insufficient to guarantee design’s adherence to RETs
  - Increasing need for more *geometry regularity by design*
Regular Logic Bricks

- Arrays offer advantages for silicon characterization and even inventory, but at a high area penalty.
- Regular Logic Bricks can offer more efficient use of area, and still provide the required regularity.

Map a simple set of logic primitives onto regular fabric patterns to form logic bricks.
Macro Regularity

- Regular fabric ensures that logic bricks share geometry regularity with all other bricks and registers
- Fabric “rules” co-optimized for memories, IPs, and bricks
- Compatible RETs and geometries at brick boundaries

Optical proximity: 
\[ r \approx 1\text{um} \]

2-3 INV on boundaries of logic bricks

Region of influence
Some Experimental Results

- Little area benefit for using more than 10 unique bricks
  - Few unique bricks allows for macro regularity and silicon validation analogous to CLBs and bit cells

- Trade-off between number of geometry patterns and area/performance

- Ideally, regular fabric synthesis tool would determine this for each design in an application-specific manner
Exploiting Regularity

- Logic regularity provides opportunities for new predictable methodologies
  1. Small library of primitives
  2. Mapping into a set of configurable pre-defined bricks

Factors $f$ & $f'$ from $F$

$G_1$ & $G_2$ are positive & negative cofactors with respect to function $f$
Ultimate Goal

- From synthesis we define the set of regular logic bricks that cover the extracted logic modules.
- From the fabrics level, perform shapes-level physical-synthesis to construct configurable bricks.
  - Nano-scale constraints allow us to simplify this shapes-level physical synthesis problem.
  - Can be optimized with simulation-based printability modeling.

Automated layout
Further Considerations

- Global effects and system-level issues
  - Memory and logic compatibility
  - Regular BEOL – structured routing
  - Analog components