Heterogeneous 3-D stacking, can we have the best of both (technology) worlds

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Corporate Vice President
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The ‘Chameleon’ Chip
Field Programmable Gate Array (FPGA)
Moore’s Law

1965: Transistor density doubles every year

Revised 1975: Transistor density doubles every two years

"Cramming more components onto integrated circuits" Gordon Moore, Electronics, Volume 38, Number 8, April 19th 1965

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A Career in One Graph

Minimum Feature Size

- 10um
- 1um
- 100nm
- 10nm
- 1nm


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Cost Comparison: Monolithic vs Multi-Die

“Moore’s Law is really about economics” – Gordon Moore

Die Cost

Die Area

Monolithic

Multi-Die
Why is First 3D Logic Product an FPGA?

- Natural partition using “long lines”
- Very low “opportunity cost”
- No 3rd party dependence
- “Size matters” to customers
- Compelling value proposition “next generation density in this generation technology”
Virtex 2000T: Homogeneous Stacked Silicon Interconnect Technology (SSIT)

FPGA Slices Side-by-Side

- Silicon Interposer
  - >10K routing connections between slices
  - ~1ns latency

FPGA slice
Elements of SSIT

- **Silicon Interposer**
- **Microbumps**
- **Through-Silicon Vias (TSV)**

- **Package Substrate**
- **28nm FPGA Slice**

- **C4 Bumps**
- **BGA Balls**

- **New! FPGA Package Interposer**

- **Passive Silicon Interposer** (65nm Generation)

- **4 conventional metal layers connect micro bumps & TSVs**

- **Access to power / ground / IOs** through silicon Vias

- **Bridging power / ground / IOs to C4 bumps**

- **Minimal heat flux issues**

- **Side-by-Side Die Layout**

- **New!**

- **FPGA Package Ball**

- **1mm**

- **0.2mm**

- **0.04mm**
3D Supply Chain

FPGA, Interposer, & Package Design

28nm FPGA & Interposer

Package Substrate

µBump, Die separation
CoC/CoWoS, & Assembly

Final Test of Packaged Part

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Co(CoS) Process Flow

1. Wafer with TSV u-pad/bump, Probe
2. Carrier
3. Carrier Mount Thin & TSV Reveal UBM & C4-bump
4. Carrier De-mount to Film frame
5. Dice
6. Interposer-on-Substrate
7. Package
(CoW)oS Process Flow-1 (Courtesy of TSMC)
(CoW)oS Process Flow-2 (Courtesy of TSMC)

1. Transfer glass to tape
   - Tape

2. Singulation
   - Tape

3. TIS (Stacking, C4)
   - Build up Subs.

4. TIS (Ring+Lid)
   - Thermal Interface
   - Metal (TIM)
   - Lid
   - Ring

Top view

Bottom view

Side view
3D Stacking: A world of difference

Earth
Area: ~500 Million km²
Population: ~6.8 Billion People
Oceans: 5
Age: ~4.5 Billion Years

Virtex-7 2000T
Interposer Area: ~775 mm²
Population: ~6.8 Billion Transistors
Sub-chips: 5
Age: ~45 weeks
Heterogeneous Integration
# 3 Decades of Microprocessor Integration

## A Personal History

> “Integrate or be integrated” – Fred Weber, former CTO AMD

<table>
<thead>
<tr>
<th>Year</th>
<th>Company</th>
<th>Product</th>
<th>Integration Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>1983</td>
<td>Harris</td>
<td>J11</td>
<td>Core L2$ North Bridge GPU</td>
</tr>
<tr>
<td>1989</td>
<td>DEC</td>
<td>Rigel</td>
<td>1.5um DP Ctl L1 $ FPU</td>
</tr>
<tr>
<td>1991</td>
<td>DEC</td>
<td>Alpha</td>
<td>0.75um</td>
</tr>
<tr>
<td>2005</td>
<td>Microsoft</td>
<td>Xenon</td>
<td>90nm 3 Core</td>
</tr>
<tr>
<td>2011</td>
<td>AMD</td>
<td>Fusion</td>
<td>40nm 2 Core</td>
</tr>
</tbody>
</table>

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## What Happened to System on a Chip?

<table>
<thead>
<tr>
<th></th>
<th>Logic</th>
<th>Memory</th>
<th>Analog</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Global Revenue 2011</strong></td>
<td>$150B</td>
<td>$68B</td>
<td>$45B</td>
</tr>
<tr>
<td><strong>Moore Scaling</strong></td>
<td>Good</td>
<td>Good</td>
<td>Poor</td>
</tr>
<tr>
<td><strong>Technology “Vintage”</strong></td>
<td>28nm</td>
<td>28nm</td>
<td>180nm?</td>
</tr>
<tr>
<td><strong>Transistor Characteristics</strong></td>
<td>High performance/ Low leakage</td>
<td>Low leakage/ moderate performance</td>
<td>Stable with good voltage headroom</td>
</tr>
<tr>
<td><strong>Metallization layers</strong></td>
<td>&gt;9</td>
<td>&lt;5</td>
<td>&lt;6</td>
</tr>
<tr>
<td><strong>Differentiators</strong></td>
<td>High density logic</td>
<td>Charge storage</td>
<td>Passives, Optical</td>
</tr>
</tbody>
</table>
What’s the Problem with Multiple Packages?

The packaging chasm
- Two orders difference in package trace/width vs silicon metallization
- I/O also isn’t scaling due to bump pitch and chip to chip loading issues
- Leads to increased area, power and complexity (SERDES)

To scale in X dimension

- Pkg via diam
- Pkg trace width
- Chip top metal

- Solder Bump
- Cu Pillar

~0.6 μm
~3 μm
~100 μm

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Chip Input/Output Bottleneck

15x drop in I/O-to-logic ratio by 2020

Source: ITRS
Crossing the Packaging Chasm

Logic Process  Memory Process  Analog Process

ARM uP

FPGA

DRAM Memory

Analog
Virtex-7 HT: Heterogeneous SerDes

- Top View
  - 28G SerDes
  - FPGA
  - TSVs
  - Fabric Interface

- Cross Section
  - 28G
  - FPGA
  - Passive Interposer
  - 13G
  - 28G SerDes

- Key Features:
  - Yield optimized
  - Noise isolation
  - 28G process optimized for performance
  - FPGA process optimized for power

- Specifications:
  - 2.8Tb/s ~3X Monolithic
  - 16 x 28G Transceivers
  - 72 x 13G Transceivers
  - 650 GPIO
7V580T – Dual FPGA Slice with 8x28Gb/s SerDes Die
Interposer Routing and DCAP

Wire coupling, no shielding

Wire coupling, with shielding

SSN, no DCAP
SSN, with DCAP

Wire Length Histogram

3mm

6mm
TSV Capacitance as Function of Substrate Resistivity

- Measured 20ohm-cm Silicon interposer
- Simulated 20ohm-cm Silicon interposer
- Measured 10ohm-cm Silicon interposer
- Simulated 10ohm-cm Silicon interposer
Insertion Loss as a Function of Interposer Resistivity

- Measured 20ohm-cm Silicon interposer
- Simulated 20ohm-cm Silicon interposer
- Measured 10ohm-cm Silicon interposer
- Simulated 10ohm-cm Silicon interposer

Frequency [GHz] vs. Insertion Loss [dB]
Simulated Eye Diagram and Measured Eye Diagram Comparison @ 28Gb/s

Measured Amplitude: 923mVp-p
Measured Total Jitter: 6.25 ps @ BER 10E-12.
Measured Random Jitter: 230 fs (0.175UI of total jitter)
3D Thermo-Mechanical Simulations at 25°C
### SSIT Enables Scalable FPGAs

<table>
<thead>
<tr>
<th></th>
<th>XC7VH290T</th>
<th>XC7VH580T</th>
<th>XC7VH870T</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Network</strong></td>
<td>2 x 100G</td>
<td>2 x 100G</td>
<td>1 x 400G or 4 x 100G</td>
</tr>
<tr>
<td><strong>GTZ (28G)</strong></td>
<td>8</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td><strong>GTH (13G)</strong></td>
<td>24</td>
<td>48</td>
<td>72</td>
</tr>
<tr>
<td><strong>Logic Cells</strong></td>
<td>284K</td>
<td>580K</td>
<td>876K</td>
</tr>
</tbody>
</table>

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Higher memory bandwidth at lower power

- 1Tbps – 2Tbps
- ~1Gb/s per interposer wire
- Simple extension of existing work
3D Active on Active: The Next Frontier

Who’s on top?

- High performance chip on top for thermal and TSV process availability
- Bottom die supports power TSV’s for top die
- Floor-planning critical
  - Thermal concerns
  - TSV keep out zones
Challenges

Cost
- Wafer backside processing is complicated
- “Device quality” wafers used for interposers
- KGD methodologies still emerging

Scalability
- Micro-bump scaling is limited
- Super-sized interposers (>30mm x 30mm)
- Improve TSV aspect ratio

Design Support
- Multi-die analysis without Multi-mode Multi-corner explosion
- Thermal modeling based on vertical hotspots
Summary

- Economic and technology forces are aligned to enable 3-D stacking

- The “end game” will see three distinct technologies: Logic, Memory, Analog

- Heterogeneous integration is already here
Thank You

Questions?
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