ON THE WAY TO PRACTICAL TOOLS FOR BEYOND DIE CODESIGN AND INTEGRATION

Honoring Prof. Yoji Kajitani 梶谷洋司先生
ISPD 2013
Experience I hope the audience to have

- Honoring Prof. Kajitani
  - By showing some traces of exploration path

- Enjoying this talk
  - Embedded 5 research problems (actually 6)
Outline

- Prof. Kajitani I know
- The beginning
  - Problem 0
- Inspirations from Prof. Kajitani
  - Problem 1
- Influences
  - Problem 2-4
- Collaboration, visit and exploration
  - Taiwan company visits and forums
  - Problem 5
- Stepping into the future of beyond die tools
Kajitani: The “Coding” Master

- Famous sequence pair representation for floorplanning/placement
  - Influenced countless researches
- Also an artist
- Very easy-going and amiable
- Likes to swim and walk very much
- Hard-working
- Many more...
The Beginning

- 2008, lucky year to me
  - Got an invitation to work together
- Why do I have this honor?
  - 2007 ASPDAC paper
  - I am Martin’s student 😊
Problem 0: Fast Flip-Chip Pin-Out Designation by Pin-Block Design and Floorplanning

R.-J. Lee and H.-M. Chen

ASPDAC 2007 and TVLSI Aug 2009
Constraints and Considerations

- **Locations of PCB components**
  - Reducing SSN noise
    
    \[
    V_{SSN} = NL_{tot} \frac{dI}{dt}
    \]
    
    \(V_{SSN}\): Simultaneous Switching Noise  
    \(N\): Number of drivers switching  
    \(L_{tot}\): Equivalent inductance in current loop
  
  - Facilitating PCB planar routing
Routing pattern on PCB and PKG

- Signal integrity issue (net balancing)
- Routability issue

**PCB board top view**
- Pad size: 14 (mil)
- Pad pitch: 39.37 (mil)
- Net on PCB (width/spacing): 5/5 (mil)
- Via: 22 (mil)

(1 mil = 25.4 um)

**Package substrate bottom view**
- Solder ball: 600 (um)
- Ball pitch: 1000 (um)
- Net width on substrate (top/bottom): 50/50 ~ 350 (um)
- Via: 350 (um)
Constraints and Considerations (cont.)

- Signal integrity issue
  - Return path pin
  - Shielding pin

\[ I_{\text{noise,}C_m} = C_m \frac{dV_{\text{driver}}}{dt} \]

- Noise induced by mutual capacitor
- \( C_m \): Mutual capacitance
## Pin Pattern Design

### Characteristics of signal-pin patterns

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Application</th>
<th>Signal-pin NO.</th>
<th>Pin-to-pin crosstalk immunity</th>
<th>Net balance</th>
<th>Signal shielding on package substrate (VDD/VSS)</th>
<th>Power delivery aware</th>
<th>Pin-designation efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Differential signal</td>
<td>16</td>
<td>Excellent</td>
<td>Good</td>
<td>Good</td>
<td>VSS</td>
<td>Without</td>
</tr>
<tr>
<td>2</td>
<td>Differential signal / Single-ended signal</td>
<td>20</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
<td>VSS</td>
<td>Without</td>
</tr>
<tr>
<td>3</td>
<td>Differential signal / Single-ended signal</td>
<td>20</td>
<td>Good</td>
<td>Not good</td>
<td>Good</td>
<td>VSS</td>
<td>Without</td>
</tr>
<tr>
<td>4</td>
<td>Differential signal / Single-ended signal</td>
<td>24</td>
<td>Excellent</td>
<td>Not good</td>
<td>Good</td>
<td>VSS</td>
<td>Without</td>
</tr>
<tr>
<td>5</td>
<td>Differential signal / Single-ended signal</td>
<td>24</td>
<td>Excellent</td>
<td>Not good</td>
<td>Good</td>
<td>VDD</td>
<td>With</td>
</tr>
<tr>
<td>6</td>
<td>Single-ended signal</td>
<td>36</td>
<td>Not good</td>
<td>Not good</td>
<td>Not good</td>
<td>None</td>
<td>With</td>
</tr>
</tbody>
</table>
Pin-Block (PB) Construction and Grouping

- PB construction ➔ PB grouping ➔ Rough PB plan
  ➔ Min. PKG size ➔ PB floorplanning ➔ Final PB plan

Floorplanning

\[
E = \begin{cases} 
< 0, & \text{Excess} \\
= 0, & \text{Exact} \\
> 0, & \text{Empty}
\end{cases}
\]
Pin-Block Construction and Grouping (cont.)

- Pin-block construction

(source: Internet)
Start to Work Together
Inspiration/Work from Collaboration

- Introducing Problem 1
  - Came from a training assignment for students

- The legacy of sequences
Problem 1: Escaped Boundary Pins Routing for High Speed Boards

C.-Y. Chin, C.-Y. Kuan, T.-Y. Tsai, H.-M. Chen, and Y. Kajitani

DATE 2010 and TCAD March 2013
Routing under Fixed-Ordering Pin Locations

- Pin sequence
  - Counterclockwise
  - Pin sequence: A B C D E

- Connected Component Point (CCP) & Dynamic Pin Sequence (DPS)
  - CCP: C
  - Pin-Seq C_1: ABCDE
  - Pin-Seq C_2: BADEC
  - DPS: ABBADECCDE

- Multiple components
  - PCB boundary
  - component pins
  - boundary pins
  - CCPs: C, G, I
  - DPS: KHHKJIJBEFGGFDDDEACCBA
Routing under Fixed-Ordering Pin Locations

- **CCP Selection**

Generation of maximum weight spanning tree. The component with the largest connectivity is chosen to be the base DPS (C_1 here).
Routing under Fixed-Ordering Pin Locations

- Against-the-wall routing (similar to Boundary Routing)

- Routing order determination (max routability)
  - Supowit’s algorithm

Either net B or net A is unroutable

corresponding circle graph
First Stage Routing: Topological

- Overall flow of the topological routing

Diagram:
- DPS generation
  - Gen Pin-Seq
  - Merging seq & CCP selection
- Decide net ordering using Supowit’s algo.
- Against-the-Wall Routing
- Any unrouted Net?
  - Yes: New layer
  - No: Done
Second Stage Routing: Length-Constraint-Aware Routing Refinement

- **Key idea**
  - Pin locations cause length differences
  - Nets are grouped into a bunch

- **Mapping pin locations to 1-D coordinates**
Length-Constraint-Aware Routing Refinement

- Formulating as ILP

against-the-wall routing results (input)

ILP refinement routing results (output)

path-equivalent constraints
position constraints
obstacle-avoid constraints

Merging tree of the ILP formulation
Routing Instance

A partial enlarged view of TestCase IV
Influences in Research

- After years of collaboration and discussion, we also come up with our own works influenced by it.

- Introducing Problems 2-4
  - Some are related to Martin’s works.
Problem 2: Board- and Chip-Aware Package Wire Planning

R.-J. Lee, H.-W. Hsu, and H.-M. Chen

IEEE TVLSI Sep 2012
Our Problem

**Input:**
- Given two sequences:
  - Die-side ordered pin sequence \((DOPS)\)
  - Package-side ordered pin sequence \((POPS)\)

**Output:**
- Pin-out designation for 2-layer BGA package
- The corresponding wire planning (monotonic global routing) for package design and PCB escape routing

**Objectives:**
- Minimize package size
- Minimize wire congestion
- Minimize wirelength variation for each layer
2-Layer BGA Model

- BGA model
  - Via in a grid pattern
  - Empty un-used slot
  - Assigned via/ball

- 2-layer package
  - Top layer: DOPS to via
  - Bottom layer: via to ball

- Printed circuit board
  - Ball to POPS
Observations

- Monotonic routing
  - Along one direction
  - No turn back
- For net1/net2
  1. (a)(e) not monotonic
  2. (b)(d)(f)(h) monotonic but use more columns
  3. (c) (g) monotonic

Rule1: assign to different row if orderings are reverse
Rule2: assign to same column to reduce package size
Interval Diagram

- Analyze DOPS and POPS
- Build an edge if ordering is reverse
Initial Pin-Out Designation
Cost Evaluation: Congestion, Length Difference, Package Size

\[ Cost_{vi/bi} = \alpha \times Cong_{vi/bi} + \beta \times Diff_{vi/bi} + \gamma \times PS_{vi/bi} \]

\[ Diff_{vi/bi} = dist(v_i/b_i) - dist(\text{avg}) \]

- Cost of via/ball
  - Calculated separately
  - Summed up in opt.

\[ cVGA = \sum_{i=0}^{n} Cost_{vi} \]
\[ cBGA = \sum_{i=0}^{n} Cost_{bi} \]
\[ Sum = cVGA + cBGA \]
Wire Planning Instance

Initial solution
Wire Planning Instance

(a) Greedy-full mode
(b) LPC-full mode

- Lower congestion
- Lower length variation
- Almost the same package size

➢ Trade-off between routability and package size
Problem 3: BGA Bump Assignment for Chip-Package Codesign

M.-L. Chen and H.-M. Chen
Problem Formulation

- **Given**
  - I/Os assignment
  - Balls assignment

- **Objective**
  - Find a solution of bump assignment
    - number of tracks on RDL routing is minimized
    - routability of package route is maximized
Simultaneous Escape Routing

- To find planar escape solutions in both components so that they are honoring the same escape ordering.

Define **routing boundary** as the boundary of the maximum routable region of the unrouted pins.

- 6 routing modes

![Diagrams showing different routing modes](image_url)
Dynamic Net Ordering

- Define routing cost vector \((\alpha, \beta)\)
  - # of pins **trapped** (unroutable) by routing current, \(\alpha\)
  - # of pins **blocked** (but still routable) by current routing, \(\beta\)

Cost of Net a: \((\alpha, \beta)\)

- Trap b: \(\alpha = 1\)
- Block c: \(\beta = 1\)
1: for each of the six routing modes do
2:   repeat
3:     for each unrouted net i do
4:       route Net i in the left component by current mode
5:       route Net i in the right component by current mode
6:       calculate the cost vector for Net i
7:       clear the routes generated for Net i
8:     end for
9:   choose the net j with minimum cost
10:  if Net j traps other nets then
11:     backtrack and reorder
12:  else
13:     route Net j in the left component by current mode
14:     route Net j in the right component by current mode
15:   end if
16:  until all nets are routed or exceed the backtrack limit
17:  store the solution for this routing mode
18: end for
19: output the solution with the best routability
What We Proposed: Using B-Escape for Package Routing

1: for each of the six routing modes do
2: repeat
3: for each unrouted net i do
4: route Net i in package by current mode
5: calculate the cost vector for Net i
6: clear the routes generated for Net i
7: end for
8: choose the net j with minimum cost
9: if Net j traps other nets then
10: backtrack and reorder
11: else
12: route Net j in package by current mode
13: end if
14: until all nets are routed or exceed the backtrack limit
15: store the solution for this routing mode
16: end for
17: output the solution with the best routability
Find bump assignment according to the package escape routing result.
Choosing a solution from bump assignment to minimize the difference between bump pin order and I/O pin order
Problem 4: Simultaneous Escape Routing for Diff Pairs and Multiple Components

C.-Y. Chin, Y.-J. Lee, and H.-M. Chen
B-Escape: Not Aware of Diff Pairs
Diff Pairs Aware B-Escape
Simultaneous Escape in Routing Multiple Components

Fig. 1. An illustration of routing problem when multiple busses of a component need to be escaped. (a) The routing result is illegal: net I belongs to B_2 but not B_1, (b) The routing result of B_1, net I is blocked, (c) The rectangle representation of the two busses, they are overlapped and cannot route in the same layer in [5]. (d) The routing result of the proposed algorithm.

1. Topological routing
2. Dynamic Routing Graph

Bus B_1 = \{A, B, C, D, E, F\} Bus B_2 = \{I, J, K\}
# of nets: 34
# of busses: 4
Visits, Forum, and Exploration

- Other attempts
  - Dr. Murata’s visit in 2008
  - 2009 Japan-Taiwan EDA Science and Technology Symposium
  - EDA forum 2010@Taiwan
  - Visits to AsRock, Faraday, GUC
    - Introducing Problem 5
Concept: Just For Feasibility Study
Taiwan EDA Forum 2010

Length Aware Routing and Clock Tree Design

Yoji Kajitani (梶谷洋司)
The university of Kitakyushu, Japan

臺灣國科客座教授（Nov. 2010-Jan. 2011）
Problem 5: PCB Routing Considering Motes
What is Mote?

- During our several visits to board design companies, we heard about power islands.
- It is called **Motes**
  - Split-plane situation
  - A total break in the copper plane, forming an isolated region
- This technique is often used to form unique power islands that connect either to a voltage different from the rest of the plane or to the same voltage through a PI filter.

Source: High-speed circuit board signal integrity by Thierauf, 2004
An increase in inductance and reduction in capacitance causes the impedance to increase. Therefore it is best to move mote-crossing signals to a routing layer that has an unbroken return path. Differential signaling is sometimes used to cross motes.
Summary
Conclusion 1

- We are on the way.?(summary of attempts I know so far)
  - Prof. Martin Wong and Prof. Kajitani in board routing
  - Prof. YW Chang and me and others in chip-package/package-board codesign
  - Prof. XL Hong and others in package routing

- Practical automation tools for board design and codesign of board/system-package-chip are hard to come by (why?)
  - Situations are very similar what we experienced in analog design automation tools
  - We can discuss offline if more people are interested

- The future of this direction
  - Based on the demands from the industry
I am really honored and happy to work with Prof. Kajitani in these years

- He is considered my another mentor in my research path: how to dedicate more in research
- I also get to know some of his students and become good friends

I really hope the people down below have enjoyed my presentation

- Let us welcome Prof. Kajitani’s intriguing talk!