Today’s Talk

1) Rect. packing-base analog placement
   ➔ Sequence-pair Packing
   ➔ Constraint-driven Optimization

2) With or without packing scenario, how do we develop analog placement?
   ➔ Analytical Analog placement with proximity constraints
   ➔ Comparison : w/ and w/o topological packing technique
INPUT: A set of rectangles, each of which has width and height
OUTPUT: A placement of rectangles
SUBJECT TO: No overlapping of any pair of rectangles
OBJECTIVE: Minimize bounding box of all the rectangles

Sequence-Pair[ICCAD95], [TCAD96]
Topological Representation and Constraint Graphs

Placement (w/o any overlapping):

- $a$ is left-of $c$ ($c$ is right of $a$)
- $b$ is left-of $c$ ($c$ is right of $b$)
- $b$ is below $a$ ($a$ is above $b$)

Constraint graphs:

- Vertical const. graph
- Horizontal const. graph

Compacted placement:

NOTE: $G_v$, $G_h$ are weighted DAG
Sequence-Pair(1)

Placement

Sequence-Pair

$SP = (\alpha, \beta) = (abcdef, bfcaed)$

$\alpha^{-1}(X)$: position of $X$ in $\alpha$

$\alpha^{-1}(X) < \alpha^{-1}(Y), \beta^{-1}(X) < \beta^{-1}(Y) \iff X$ is left-of $Y$

$\beta^{-1}(X)$: position of $X$ in $\beta$

$\alpha^{-1}(X) > \alpha^{-1}(Y), \beta^{-1}(X) < \beta^{-1}(Y) \iff X$ is below $Y$
Sequence-Pair(2)

Gh: horizontal constraint graph  Gv: vertical constraint graph

\[
\begin{align*}
S_h & \rightarrow a \rightarrow d \rightarrow T_h \\
& \rightarrow b \rightarrow c \rightarrow e \\
& \rightarrow f
\end{align*}
\]

\[
\begin{align*}
T_v & \rightarrow a \rightarrow d \\
& \rightarrow b \rightarrow c \\
& \rightarrow e \\
& \rightarrow f \\
S_v
\end{align*}
\]

\[
\begin{align*}
X & \rightarrow Y \\
W(X)/2 + W(Y)/2
\end{align*}
\]

\[
\begin{align*}
Y & \rightarrow X \\
H(Y)/2 + H(X)/2
\end{align*}
\]

NOTE: w(X), h(X): width, height of X
1. Every placement corresponds to a sequence-pair

2. Packing according to constraint graphs can generate a minimal area placement under the same topological description

3. A solution space induced by sequence-pairs always includes an optimum placement with respect to area
Sequence-Pair(4)

Application to simulated annealing

Moves:

1. FullExchange$(a, b)$:

2. HalfExchange$(a, b, \beta)$:
Practical Applications of Packing

• Building block placement
• Floorplanning for large scale circuits
• Analog placement
• 3D Cube packing
• Polygon packing
• Scheduling for dynamic reconfigurable system

...
Analog Placement

Device Generation  Cell Design  Block Design

Each Placement…

1. Circuit netlist
2. Design rule
3. Specification / constraints

Layout
(Layers w/ Geometry, Contacts, Wires...)

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Analog Placement

• Geometry-based placement
  – ILAC [CICC88], KOAN/ANAGRAM [ICCAD88]
    → larger area and time consuming

• Topology-based placement (modern)
  – BSG, Sequence-Pair, O-tree, B*-tree, TCG-S, ...
    – Constraint-driven
      • symmetry, common-centroid, alignment and others
    → smaller area and rapid convergence
Constraint-driven Placement

1. Formulation as a rectangle packing problem
2. Extensions under constraints
   ● Separation Constraint
   ● Alignment Constraint
   ● Abutment Constraint
   ● Boundary Constraint
   ● Symmetry Constraint
   ● Preplaced Constraint
   ● Range Constraint
   ● Cluster Constraint
Our Works in Constraint-driven Analog Layout

- **Placement**
  - ASPDAC04, GLSVLSI04, IEICE04, ISVLIS06a, ASPDAC09, ASPDAC08
  - AMPER produced by JEDAT

- **Routing**
  - GLSVLSI05, IEICE06

- **Compaction**
  - ASPDAC02, ISVLSI06b
  - GRANA produced by JEDAT

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Analog Constraint Formulation

**Separation Constraint**

![Separation Constraint Diagram]

horizontal constraint graph:

maximal separation

\[ w(B, \text{pdf})/2 + w(C, \text{poly})/2 + 0.85 \]

**Alignment Constraint**

![Alignment Constraint Diagram]

sequence-pair condition:

\[ \alpha^{-1}(A) < \alpha^{-1}(B), \beta^{-1}(A) < \beta^{-1}(B) \]

bottom-alignment

\[ (B-A)/2 \]

vertical constraint graph:

\[ h(B)/2 - h(A)/2 \]

**Abutment Constraint**

![Abutment Constraint Diagram]

sequence-pair condition:

\[ \alpha^{-1}(X) < \alpha^{-1}(A) \]

vertical constraint graph:

\[ \min(h(A), h(B))/2 - \max(h(A), h(B))/2 \]

**Symmetry Constraint**

![Symmetry Constraint Diagram]

sequence-pair condition:

\[ \alpha^{-1}(A) < \alpha^{-1}(B) \iff \beta^{-1}(\text{sym}(B)) < \beta^{-1}(\text{sym}(A)) \]

horizontal constraint graph:

\[ w(A)/2 + d_1 \]

vertical constraint graph:

\[ w(B)/2 + d_2 \]

NOTE: X is dummy node, d_1, d_2 should be precalculated
Objective and Optimization

- **Objective**: Area + Wirelength (HPWL or MST)

- **Framework**: Simulated Annealing
  - **Moves**
  - **Feasibility Check**
    - Topological Checking $\rightarrow$ sequence-pair conditions
    - Geometrical Checking $\rightarrow$ no positive cycle
Design Flow for Analog Layout

- Schematic Entry
  - Netlist Generation
  - Simulation & Device Sizing
- Device Generation
- Layout Constraint Generation
- Constraint-Driven Placement
- Routing
- DRC, LVS
- Compaction (option)

LPE & PostLayout Simulation
Design Case Study: LCD-Driver

NOTE: Both ICs by ‘manual’ and ‘const-driven’ implemented on NECEL 0.35um, both of them could work. (Collaboration with NEC micro systems.)
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Representation of Placement (1)

(1) Schematic

(2) Symbolic/Topological Placement

(3) Physical/Geometrical Placement

(4) Electrical Placement
Representation of Placement (2)

Schematic  Topological Placement  Geometrical Placement  Electrical Placement

Outputs
- Outline
  - I/O pin
  - Device size
- Layers
  - Design rules
- Parasitics

Steps
- Device sizing
- Floorplanning
- Device Generation (PDK)
- Layout (Placement/Routing/Compaction)
- LPE

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# Optimization of Placement

**Constraint-driven**

1. Spec.: $V_{off} < 1\text{mV}$
2. Extract diff. pair (A, B)
3. Symm. Const.: A and B is x-symmetry for X
4. Represent placement and constraint topologically
5. Search optimal placement under constraints

**Sensitivity-driven**

1. Spec.: $V_{off} < 1\text{mV}$
2. Generate parasitic network
3. Sensitivity analysis
   $$\min\left(\frac{\partial V_{\text{offset}}}{\partial X_A} + \frac{\partial V_{\text{offset}}}{\partial X_B} + \frac{\partial V_{\text{offset}}}{\partial X_C}\right)$$
4. Perturb placement of A, B, C and optimize placement

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Constraint-driven v.s. Sensitivity-driven

Constraint-driven

- Need to substitute objective and constraints
- Available to use general optimizer like SA
- Rapid computation and global optimization
- EDA and users can have explicit consensus by means of constraints

Sensitivity-driven

- Directly optimize specification without substituting objective and constraints
- Huge computation and local optimization
- All can be done in EDA
- Need routing information for accuracy
Preliminary of Sensitivity-driven: Analytical Analog Placement

Analytical Placement
Pros: high speed, good scalability
Cons: many overlaps, messy

Proximity function induced by group information

Analytical analog placement w/ proximity constraints
1. Extract sub-netlist corresponding to current mirror, differential pair, logic primitive...

2. Place blocks corresponding to sub-netlists.
w/o Rect. Packing: Analytical Formulation

Min: CostOfHPWL + CostOfOverlap + CostOfGroupProximity

Variables: x and y-coordinates of each cell

CostOfHPWL $\rightarrow$ LogSumExp.

CostOfHPWL $\rightarrow$ Overlap Removal Length, Takashima, et. al. SASIMI 2010.

CostOfGroupProximity $\rightarrow$ like an HPWL formulation.

Well Group: P-well, N-well with same potential
CM. Group: current mirrors
DP. Group: differential pairs
Signal Group: path from VDD to GND
Cap. Group: capacitances with same size
Res. Group: resistors connected in parallel or serial.
Group Proximity Cost Formulation

\[ \text{GroupCost} = \max(\text{AreaOfBoundBox, SumOfCellArea}) \]

Group : \{ A, B, C, D, E, F, G, H \}

\[ x_{\min} = t \times \log \exp \left( \frac{1}{t} \right) \]
\[ i \in \{ A, H \} \]

\[ x_{\max} = t \times \log \exp \left( \frac{r(i)}{t} \right) \]
\[ i \in \{ A, H \} \]

\[ t \times \log \left\{ \exp \left( (x_{\max} - x_{\min}) \times (y_{\max} - y_{\min}) / t \right) + \exp \left( \frac{a(i)}{t} \right) \right\} \]
\[ i \in \{ A, \ldots, H \} \]
Example: Analytical Analog Placement w/ proximity constraints

TIME : 1.0 sec.
AREA : 29,793 (100%)
HPWL : 2,998 (100%)

But, many DR-errors.
Analytical Analog Placement w/o Proximity Constraints

TIME : 1.0 sec.
AREA : 22,637 (76%)
HPWL : 4,259 (142%)
Eliminating DR-errors

De-compaction
No DR-errors.

1D-Compaction
No DR-errors.
w/ Rect. Packing: Multi-output Floorplan

- Circuit Netlist w/ Device Configuration
- Floorplan
- FP
- FP
- FP
- Diffusion/Gate-sharing
- Routing
- Layout
- Layout
- Layout
- Designer’s Choice
- Parameter Tuning

Redesign of Netlist or Regeneration of Devices
Comparison:
Rect. Packing-base Placement (1)

<table>
<thead>
<tr>
<th>AREA</th>
<th>HPWL</th>
<th>DR-errors</th>
</tr>
</thead>
<tbody>
<tr>
<td>23,212 (78%)</td>
<td>3,443 (115%)</td>
<td>No DR</td>
</tr>
<tr>
<td>25,405 (85%)</td>
<td>4,010 (134%)</td>
<td>No DR</td>
</tr>
</tbody>
</table>

Total time for 10 placements: 7.0 sec.
Comparison:
Rect. Packing-base Placement (2)

AREA : 27,070 (91%)
HPWL : 3,814 (127%)
No DR-errors.

AREA : 26,798 (90%)
HWPL : 4,083 (136%)
No DR-errors.
Diffusions (gates) can save area if they have the same net.

**Possible gate/diffusion sharing:**
A set of blocks forming a topological row and array.
Different rules for separation between wells

A and B have the same potential → separation = ws1

A and B have the same well island → separation = ds2 not for wells but diffusion

A and B have different potential wells → separation = ws3

possible well-island:
a set of blocks which are rectangular extractable
Control of Adjacency: Diffusion Sharing

w/o diffusion sharing  w/ diffusion sharing
Summary

- Rect. Packing:
  - Compacted
  - Multi-output
  - Soft modules
  - No DR errors
  - Easy to take constraint-driven
  - Easy to control adjacency (constraints)
  - Floorplan to estimate area

- Analytical:
  - Less wire-length
  - Quick
  - Scalability
  - Potentially applicable to sensitivity-driven
  - Initial placement for manual designer
Thank you!
Analog Layout Constraint

- **Netlist**
  - PWR/GND
  - Hierarchical Structure
  - Differential Pair,
  - Current Mirror, …
  - Logic (INV, NAND, …)

- **IP**
  - Know-how
  - Template

- **Floorplan**
  - Block Size
  - Well Island
  - Diffusion Sharing
  - Multiplier/Finger

- **Process variation**
  - $\sigma(\Delta V_{th})$, $\sigma(\Delta \beta)$, $\sigma(\Delta \lambda)$
  - Distance-Dependent
  - Size-Dependent

- **Sim. report**
  - Sensitivity
  - Parasitics

**Constraint**
- Guard-Ring
- Dummy
- Pair / Array
- Symmetry
- Group

**Constraint-Driven Layout System**

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Separation Constraint

NOTE: \( w(X, L) = \text{width of layer } L \text{ of device } X \)

**horizontal constraint graph:**

- \( w(A, \text{pdiff})/2 + w(B, \text{pdiff})/2 + 1.5 \)
- \( w(B, \text{pdiff})/2 + w(C, \text{poly})/2 + 0.85 \)
- \( w(C, \text{poly})/2 + w(D, \text{poly})/2 + 0.45 \)

**maximal separation**

- \( w(A, \text{pdiff})/2 + w(B, \text{pdiff})/2 + 1.5 \)
- \( w(B, \text{pdiff})/2 + w(C, \text{poly})/2 + 0.85 \)
Alignment Constraint

sequence-pair condition:

\[\alpha^{-1}(A) < \alpha^{-1}(B), \beta^{-1}(A) < \beta^{-1}(B)\]
\[\text{or} \quad \alpha^{-1}(B) < \alpha^{-1}(A), \beta^{-1}(B) < \beta^{-1}(A)\]

SP=(…A…B…, …A…B…)  
SP=(…B…A…, …B…A…)

vertical constraint graph:

h(B)/2-h(A)/2  
h(A)/2-h(B)/2  
h(B)/2-h(A)/2  
0  
-0
Abutment Constraint

**sequence-pair condition:**

\[ \alpha^{-1}(A) < \alpha^{-1}(B), \beta^{-1}(A) < \beta^{-1}(B) \]

and

\[ \alpha^{-1}(X) < \alpha^{-1}(A) \text{ or } \alpha^{-1}(B) < \alpha^{-1}(X) \]

or

\[ \beta^{-1}(X) < \beta^{-1}(A) \text{ or } \beta^{-1}(B) < \beta^{-1}(X) \]

for \( \forall X (\neq A, B) \)

**vertical constraint graph:**

\[ \min(h(A), h(B))/2 - \max(h(A), h(B))/2 \]

and

\[ \min(h(A), h(B))/2 - \max(h(A), h(B))/2 \]
Boundary Constraint

sequence-pair condition:

\[ \alpha^{-1}(A) < \alpha^{-1}(X) \text{ or } \beta^{-1}(A) < \beta^{-1}(X) \text{ for } \forall X (\neq A) \]

\[ \alpha^{-1}(X) < \alpha^{-1}(B) \text{ or } \beta^{-1}(B) < \beta^{-1}(X) \text{ for } \forall X (\neq B) \]

horizontal constraint graph:

vertical constraint graph:
Range Constraint

horizontal constraint graph:  vertical constraint graph:

NOTE: P, Q are dummy blocks
range const. \(\rightarrow\) preplaced const. if P and Q are the same as A
Symmetry Constraint

**sequence-pair condition:**

\[ \alpha^{-1}(A) < \alpha^{-1}(B) \iff \beta^{-1}(\text{sym}(B)) < \beta^{-1}(\text{sym}(A)) \]

**horizontal constraint graph:**

**vertical constraint graph:**

**horizontal symmetry group**

pair-symmetry: (A,C), (B,D)

self-symmetry: E

NOTE: sym(A)=C, sym(B)=D, sym(E)=E

NOTE: X is dummy node, d1, d2 should be precalculated
Cluster Constraint(1)

Horizontal-Convex:
For any pair \((a, b)\) in \(X\) such that “a” is left-of “b”:
Any device “c” such that
“a” is left-of “c” and “c” is left-of “b” also belongs to \(X\)

Horizontal-convex

\[ a, b, c \in X \]

Not Horizontal-convex

\[ a, b \in X, c \notin X \]
Cluster Constraint(2)

X is Convexly left-of Y:
• X and Y are horizontal-convex
• No pair (a, b) such that a ∈ X is right-of b ∈ Y

X is convexly left-below Y:
• X is convexly left-of and convexly below Y
• No pair (a, b) such that a ∈ X is right-of and above b ∈ Y
Cluster Constraint (4)

sequence-pair condition for all convex relation

<table>
<thead>
<tr>
<th>X is convexly ... Y</th>
<th>Sequence-Pair ( \forall a \in X ) and ( \forall b \in Y )</th>
</tr>
</thead>
<tbody>
<tr>
<td>left-of</td>
<td>( { \alpha^{-1}(a) &lt; \alpha^{-1}(b) } \cup { \beta^{-1}(a) &lt; \beta^{-1}(b) } )</td>
</tr>
<tr>
<td>below</td>
<td>( { \alpha^{-1}(a) &gt; \alpha^{-1}(b) } \cup { \beta^{-1}(a) &lt; \beta^{-1}(b) } )</td>
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</tr>
<tr>
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<td>( \alpha^{-1}(a) &gt; \alpha^{-1}(b) )</td>
</tr>
<tr>
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<td>( \beta^{-1}(a) &gt; \beta^{-1}(b) )</td>
</tr>
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