Clock Enable Timing Closure Methodology

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Agenda

- Basics of Clock Gating
- Fixing Clock Enable Timing in RTL-2-GDSII Flow
- Results
- Conclusion
Clock Gating Basic

- Use internal (or external) signal to disable clock

- This saves Dynamic Power

- A must for low power design

- Creates new timing paths
Two Types of Clock Gating

- Using AND gate
- Using ICG Cell

Rest of presentation is about ICG type clock gating
Register to Register Path

Check Setup-hold

Check Clock-Skew
Register to Register Path with Clock Gating

- CE Path: 1ns
- CE clk Path: 0.5ns
- Clock gated clk Path: 1ns

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What is different about CE path

- Not noticed at Synthesis
- Timing available is less than cycle time
- ICG cells are not skew balanced with registers
- Violations are seen only after Clock Tree Synthesis
- Mostly affects timing critical blocks
Effect of ICG Cells Location in Clock Tree

CLK

0ns 0.25ns 0.5ns 0.75ns 1ns

Architectural Gaters

Potential bad Location CE timing

Acceptable Location

Good Location

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What to Do at RTL Level

• CE signal should be generated in the same module

• Generate CE signal from functionally related modules

• Simplify the logic that generates CE signal
CE Timing at Synthesis Step

- Reduce cycle time to ICG cells

```python
set_clock_latency  - (cycle_time/2) \ 
[get_pin all_clock_gating_registers/CK]
set_clock_latency  0  [get_pin all_clock_gating_registers/ECK]
```

- Set high setup time on ICG cells

```python
set timing_scgc_override_library_setup_hold true
set_clock_gating_style  -setup 400ps clock_gate
```

- Turn off bus sharing in Power Compiler

```python
set_clock_gating_style  -no_sharing
```
CE Timing at Floorplan Step

- When placing modules, pay attention to CE signal connectivity
- If CE signal(s) are input pins, place them close to modules that receive it

![CE timing problem](image1)
![Good CE timing](image2)

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CE Timing at placement Step

- Tightening available cycle time by changing ICG setup time

```plaintext
set timing_scgc_override_library_setup_hold true
set_clock_gating_style -setup 400ps clock_gate
```

- Tightening available cycle time by changing ICG clock latency

```plaintext
set_clock_latency -(cycle_time/2) \ 
[get_pin all_clock_gating_registers/CK]
set_clock_latency 0  [get_pin all_clock_gating_registers/ECK]
```
CE Timing at placement Step (cont)

- Create group path and add extra weight

```bash
group_path -weight 5 -name CLOCK_ENABLE \\
-to [get_cell */*GATE_LATCH]
```

- Place ICG cells close to flops

```bash
setplacer_disable_auto_bound_for_gated_clock false
```
How to Select Latency?

• Apply global latency
  – Easy, Not very efficient

• Apply based on ICG depth and fanout
  – Less depth – more latency
  – More fanout – more latency

• Apply based on CTS results
  – More accurate
CE Timing at Clock Tree Synthesis

• Clone ICG Cells

```plaintext
set icg_cells { icg_cell_1 icg_cell_2 }

split_clock_net -objects [get_cells $icg_cells] \ 
-\split_intermediate_level_clock_gates -gate_sizing

remove_ideal_network [all_fanout -flat -clock_tree]
remove_propagated_clock *
remove_clock_tree
```
ICG Cloning

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CE Timing at Clock Tree Synthesis
Cloning based on fanout and slack

foreach_in_collection CELLS [get_cells * -hier -filter "ref_name =~ *ICG*"] {

    set names [get_object_name $CELLS]
    set ckPins [get_object_name [get_pins -of_object [get_cells $CELLS] \
             -filter "full_name =~ */CLK"]]
    set eckPins [get_object_name [get_pins -of_object [get_cells $CELLS] \
             -filter "full_name =~ */ENABLE_CLK"]]
    set eckFanout [sizeof_collection [all_fanout -from [get_pins $eckPins] -flat]]
    set cgSlack [get_attribute [get_pins ${names}/ENABLE] max_slack]
    if {$cgSlack > -0.150 && $eckFanout > 100} {
        echo "${names}/E"
    }
}

remove_propagated_clock *
remove_clock_tree
CE Timing at Clock Tree Synthesis
Two Pass Flow

1. Placement
2. Clone clock tree
3. Write Verilog
4. New Placement
5. Clock Tree Synthesis
Agenda

• Basics of Clock Gating
• Problems Created by Clock Gating
• Fixing Clock Enable Timing in RTL-2-GDSII Flow
• Results
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Die Temperature Without and With Clock Gating

Relative POWER5 processor temperature (Celsius)  
- without clock gating (left) and with clock gating (right)

ICG Cells and Flops Autobound
Comparing Latency Schemes

Path

CE violation (ns)

0
1
2
3
4
5
6
7
8
9
0
100
200
300
400
500
600
700
800
900
Selective latency
1ns latency
Baseline run
Results – Effect on cloning on latency

With Cloning

Without Cloning

Paths (Sorted, low to high)
Clock Subtree After Cloning

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Comparing Single Pass and Two Pass flow

place_opt
clock_opt

place_opt
clock_clone
new place_opt
clock_opt
Different schemes to minimize latency
Conclusion

• Clock gating is requirement for low-power design

• Closing CE timing requires to pay attention at all stages of design

• By planning at every step, CE timing can be closed in high-speed low-power designs
Thank You!
Battery Life is Important

Smartphone power for continuous web access

http://www.phonesreview.co.uk/2012/09/26/iphone-5-vs-samsung-galaxy-s3-battery-life-confrontation/
How to Minimize Power

- Use process designed for low power
- Use low power architecture
- User power-gating
- Use Clock-gating
Power Saving Opportunity

Clock Gating

- System Algorithm
- System Architecture
- RTL
- Gate Level
- GDSII
Few Facts About Clock Tree Power

• 20% to 40% Dynamic power is consumed by clock tree

• About 80% clock tree power is consumed last stages of clock tree

Ref – ISPLED, 2008
Architectural/Corse Grain Clock Gating

USB_CLOCK

Control Logic

Clock_EN
en_usb_0

USB-0

Clock_EN
en_usb_1

USB-1

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Automated/Fine Grain Clock Gating
Example of Automated/Fine Grain Clock Gating

Report: clock_gating
    -nosplit
Design: red_blk
Version: F-2011.09-SP5-1
Date: Fri Aug 17 23:27:06 2012

Clock Gating Summary

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Clock gating elements</td>
<td>3133</td>
</tr>
<tr>
<td>Number of Gated registers</td>
<td>26738 (76.90%)</td>
</tr>
<tr>
<td>Number of Ungated registers</td>
<td>38077 (23.10%)</td>
</tr>
<tr>
<td>Total number of registers</td>
<td>164815</td>
</tr>
</tbody>
</table>
What To Look For In ICG

- Too many flops used for generating CE signal
- Large delay in combinational path
- Generating flops placed away from ICG cells
- Flops used to generated ICG signal placed away from each other
- Too many flops receive gated clock
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