3D VLSI: Next Generation
3D Integration Technology

Karim Arabi
Vice President, R&D
Continued smartphone momentum
World’s largest technology platform

~8B

Cumulative smartphone unit shipments forecast between 2014-2018

Source: Gartner, Sept ’13

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Mobile scale
Cumulative global unit shipments, 2013–2017

Smartphones & Tablets

PCs
Vehicles
Digital media adapters
Digital video recorders
Portable game consoles
Portable media players
Audio systems
Blu-ray disc players
Digital cameras
Game consoles
Flat-panel TVs
Set-top-boxes

Sources: Smartphones, tablets and PCs: Gartner, Sep. ’13; Vehicles: ABI, Apr. 2013; All others: Strategy Analytics, Mar. ’13

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Cloud and Mobile Computing

Big Data and abundant computing power are pushing computing to the Cloud.

Instant Data generated by sensors and users are pushing computing to the Edge.
Mobile Heterogeneous Compute Units to Lower Power

Key Drivers
- Mobile Computing
- Cloud Computing
- Big Data Analytic
- Deep Learning
- Machine Learning

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## CMOS Scaling Outlook – The Roadmap Ahead

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<tbody>
<tr>
<td>Vdd</td>
<td>1.0/0.9V</td>
<td>0.9/0.8/0.7V</td>
<td>0.7/0.6V</td>
<td>0.6V</td>
<td></td>
<td></td>
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<tr>
<td>Transistor</td>
<td>Planar/Tri-gate, Si channel</td>
<td>FinFET, Si/SiGe/Ge</td>
<td>FinFET, Si/SiGe/Ge</td>
<td>FinFET/Nanowire SiGe/Ge/III-V?</td>
<td>Tunnel FET SiGe/Ge/III-V?</td>
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</tbody>
</table>

**Technology:**
- **Planar bulk RMG**
- **Tri-gate, FinFET Si**
- **FinFET Si/SiGe/Ge channel**
- **FinFET III-V channel**
- **Nanowire, horizontal**
- **Nanowire, vertical?**
- **Tunnel FET, vertical?**

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Potential Issues to Address for 7nm and Beyond:
- FinFET/NWFET self-heating (phonon confinement)
- Feasibility of TFET and vertical channel devices
- System performance degradation (contact/BEOL bottleneck)

More Moore
- Nano-wire
- TFET
- Ge/III-V

The 3rd Dimension
- 3DVLSI (3DV)
- MRAM & RRAM
Introduction: TSV-based 3D ICs

- TSV-based 3D ICs are close to market

- TSV-based 3D ICs shortens the interconnects, still quite large (5-10um, C=10-30fF)

IBM (VLSI 2011)

TSMC (ISPD 2014)

Courtesy Panth et al., ISLPED’14
3D VLSI - An Emerging 3D Technology

3D VLSI SRAM
Samsung (2010)

3D VLSI for general logic
LETI (2011)

Vertical via
Gate

High quality thin silicon (single crystal)

(a) Gate-Level F2B
(b) Gate-Level F2F

Courtesy Panth et al., ISLPED’14
3D VLSI: Face-to-Back Fabrication Process

Bottom tier is created as usual

Thin Si layer is attached

Fabricate top-tier devices + interconnects

Courtesy Panth et al., ISLPED'14
3D VLSI: Face-to-Face Fabrication Process
Design Styles Available in 3D VLSI (1/2)

- **Transistor-level** [1]
  - Each standard cell is folded
  - Pin density increases significantly
  - Footprint reduction is ~40%, not 50%
  - Standard cell re-design required

- **CELONCEL** [2]
  - Gate-level, but cell redesign required
  - Simplified design flow
  - Same disadvantages as transistor-level


Courtesy Panth et al., ISLPED’14
Design Styles Available in 3D VLSI (2/2)

- **Block-level** \(^1\)
  - Functional blocks are 2D & they are floorplanned on to a 3D space
  - Reuse of IP
  - Does not fully take advantage of the high density offered by M3D

- **Gate-level**
  - Use existing standard cells & place them in 3D
  - Reuse of cells

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Courtesy Panth et al., ISLPED’14
Block-Level 3D VLSI Physical Implementation
Sequential 3D: Source of Inter-Tier Performance Variation

- Process improvement: < 625°C without performance loss → still too high for Cu interconnect

- Preventing damage to interconnects – Two options:
  - Use Tungsten (W) on the bottom tier → Worse interconnects on bottom tier
    - Identical devices on both tiers
  - ~ 450°C processing on the top tier → Worse transistors on the top tier
    - Identical interconnects on both tiers

- FEOL processing of top tier
  - RTA at 1200°C will damage both devices and interconnects

Courtesy Panth et al., DAC’14
Degraded Transistors

- PMOS worsens by 27.8% and NMOS worsen by 16.2% (TTm20p corner)

![Graph showing change in delays of select standard cells]

Change in delays of select standard cells

Identical devices, but W interconnect

[1] Low Thermal Budget Processing for Sequential 3D IC Fabrication, Rajendran et al., TED, 2007

Courtesy Panth et al., DAC’14
Design Flow

- RTL
- Synthesis
- Floorplanning
- Vertical Via Planning
- P&R of all blocks/tiers
- GDSII
- 3D Timing and Power Analysis
- Derive WLM

Feedback loop

Determine the block outlines in a 3D space

Determine block pin and vertical via locations

Final signoff analysis

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Variation-Aware 3D Block-Level Floorplanning

- Block Timing Constraints
- Normal/Degraded Libraries

Block Synthesis

Block flavors

Performance-aware floorplanner

\[ Cost_{VA} = \alpha \cdot WL + \beta \cdot Area + \gamma \sum_{i=1}^{N_{Block}} LPD(b_i) \]
Power-Performance Study: Identical Tier Performance

- Ideal: Zero RC for inter-block nets: **Best possible block-level implementation**

M3D closes 37% of the performance gap to ideal

M3D closes 41% of the power gap to ideal

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Power-Performance Study: Identical Tier Performance

- Similar results for all benchmarks
- 3D closes the power gap to ideal by at least 40%
- 3D closes the performance gap to ideal by up to 50% and 40% on average

Courtesy Panth et al., DAC’14
Variation-Aware Power-Performance Results

- Dashed lines = no variation-aware floorplanning
- Solid lines = variation-aware floorplanning

Courtesy Panth et al., DAC’14
Variation-Aware Power-Performance Results

- Variation-aware floorplanning always gives better results
- W on the bottom tier seems to be the best option

Courtesy Panth et al., DAC’14
Summary of Results

**Iso-power frequency**

3D closes a significant portion of the gap to ideal

**Iso-frequency power**

W interconnects have marginal overhead

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Gate-Level 3D VLSI Physical Implementation
Initial Work in Gate-level 3D VLSI

- Placement-driven partitioning using academic placers \[1\]

First, make the 3D footprint 50% of 2D

In a 2D placer, double the placement capacity of each global bin (for two-tier)

Partition the design, maintaining local area balance within each partitioning bin

“Placement-driven Partitioning”


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“Shrunk 2D” Placement using a Commercial Tool

- In a commercial tool, we cannot “double” the supply.
- Instead, we first halve the std. cell areas (multiply W/H by 0.707)

Note: We do not touch the .lib file → Timing information is maintained

W = 0.707 * W2D

Original 2D Std. Cells  →  Shrunken 2D Std. Cells

Shrunk 2D Placement → Cell Expansion → Placement-driven Partitioning

Courtesy Panth et al., ISLPED’14
Handling Memory Macros: Issues

- Memory is usually pre-placed before placement starts
  
  ![Tier 0](image)
  ![Tier 1](image)

- We cannot simply superimpose them before feeding it to the commercial tool for shrunk 2D P&R
  
  ![Shrunken Footprint](image)

This will cause a placement blockage in these regions, which is wrong.

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Handling Memory Macros: Decomposition

- Memory macros can be thought of as a combination of a placement blockage and memory pins

```
Memory pins
```

```
Memory
```

```
Placement blockage + Blockage over the memory footprint
```

```
Memory Pins
```

- If we can isolate each component, then they can be handled separately during shrunk 2D P&R

 Courtesy Panth et al., ISLPED’14
Handling Memory Placement Blockages (1/2)

- Consider the two memory regions overlapping as shown earlier

This region has memory in both tiers

After partitioning, neither tier will contain cells

Therefore, it will be a full placement blockage in the shrunk 2D footprint

These regions have memory in one tier only \( \rightarrow \) The other tier can contain cells

If the target density = 70% in the final 3D design, we set the max density of these regions = 35% (=70% once cells are expanded back to original area)

This can be achieved by creating a partial placement blockage in these areas

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Handling Memory Placement Blockages (2/2)

Partial Blockage

Pre-Placed Memory

Projected Memory Locations

Tier 0

Tier 1

Pre-placed Memory

Memory Projection

Memory Blockage Extraction

Full Blockage

Partial Blockage

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Design Flow Screenshots

Tier 0

Pre-Placed Memory

Tier 1

Full Blockage
Memory Pins
Partial Blockage

Memory Projection

Reduced Placement Density over partial blockages

Shrunk 2D P&R

Tier Partitioning

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Design Flow

Shrunken 2D

- Placement
- Pre-CTS Optimization
- CTS
- Post-CTS Optimization
- Routing
- Post-route Optimization

- Tier Partitioning
- MIV/F2F Insertion
- Tier-by-tier Route
- Tier-by-tier RC Extraction
- 3D Timing & Power Analysis

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Matching Wire Parasitics between Shrunk 2D and 3D

- Consider two cells connected to each other in Shrunk 2D & then in 3D

  \[ L_{S2D} = L_x + L_y \]

  \[ L_{3D} = L_x + L_y + L_{MIV} \]

- But \( L_{MIV} < 1\mu m \). Therefore \( L_{S2D} \approx L_{3D} \)

- However, the wire widths are different; \( W_{S2D} = 0.707 W_{3D} \)

- Since we want \( R_{S2D} \approx R_{3D} \) and \( C_{S2D} \approx C_{3D} \), we do not scale the per-unit-length RC values in the cap table file for shrunk 2D design.

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Vertical Via Insertion (Face-to-Back)

- Trick the commercial router into inserting MIVs for us \[1\]

LEF files are modified for 3D

Route with Encounter

Routing blockage to prevent MIV insertion

All gates are then placed in the same placement layer

Create separate verilog/DEF for each tier


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Vertical Via Insertion (Face-to-Face)

LED files are modified for 3D

Reverse the order of metals in Tier 0

All gates are then placed in the same placement layer

Do not add any routing blockage to prevent F2F insertion over cells

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F2B / F2F MIV Insertion Screenshots

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Single vs. Multiple MIV Insertion: Screenshots

- Conventional 3D flows have a tier-by-tier optimization step
- It is very difficult to derive timing budgets for multiple MIVs per net
- Shrunk 2D flow enables multiple MIV insertion \(\rightarrow\) Lower WL and power

![Single MIV Insertion vs. Multiple MIV Insertion](image)

Courtesy Panth et al., ISLPED’14
## Single vs. Multiple Vertical Via Insertion: Results

<table>
<thead>
<tr>
<th></th>
<th>F2B 3D</th>
<th></th>
<th>F2F 3D</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Single</td>
<td>Multiple</td>
<td>Single</td>
<td>Multiple</td>
</tr>
<tr>
<td>Total WL (m)</td>
<td>15.61</td>
<td>14.29 (-8.43%)</td>
<td>15.44</td>
<td>13.89 (-10.05%)</td>
</tr>
<tr>
<td>#MIV/F2F</td>
<td>106k</td>
<td>235k (+120.44%)</td>
<td>106k</td>
<td>202k (+89.72%)</td>
</tr>
<tr>
<td>Total Power (mW)</td>
<td>534.10</td>
<td>522.10 (-2.25%)</td>
<td>538.30</td>
<td>524.00 (-2.66%)</td>
</tr>
<tr>
<td>Cell Power (mW)</td>
<td>126.90</td>
<td>126.10 (-0.63%)</td>
<td>127.30</td>
<td>126.40 (-0.71%)</td>
</tr>
<tr>
<td>Net Power (mW)</td>
<td>293.90</td>
<td>282.70 (-3.81%)</td>
<td>297.80</td>
<td>284.30 (-4.53%)</td>
</tr>
<tr>
<td>Leak. Power (mW)</td>
<td>113.30</td>
<td>113.30 (+0.0%)</td>
<td>113.30</td>
<td>113.30 (0.00)</td>
</tr>
</tbody>
</table>

Courtesy Panth et al., ISLPED’14
3D Clock-Tree Synthesis

Traditional 3D CTS: Source-level

One clock-tree per clock-gating group in each tier, tied together at the root level.

Proposed 3D CTS: Leaf-level

Keep the entire backbone on one tier. Only insert clock MIVs to connect the FF on different tiers at the leaf level.

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Leaf-Level CTS: Screenshots

Clock backbone on Tier 0

Zoom in of red rectangle

Leaf clock net on Tier 0

Clock backbone

Leaf clock net on Tier 1

Leaf buffer

Flip-Flop

Clock MIV

Courtesy Panth et al., ISLPED’14
## CTS Results

<table>
<thead>
<tr>
<th></th>
<th>F2B 3D</th>
<th>F2F 3D</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Source-level</td>
<td>Leaf-level</td>
</tr>
<tr>
<td>#Vertical Via</td>
<td>871</td>
<td>11,376 (+1.2k%)</td>
</tr>
<tr>
<td>Clock Skew (ps)</td>
<td>197.42</td>
<td>103.00 (-47.83%)</td>
</tr>
<tr>
<td>Clock Power (mW)</td>
<td>68.40</td>
<td>48 (-29.82%)</td>
</tr>
<tr>
<td>Clk WL – Tier 0 (m)</td>
<td>0.55</td>
<td>0.62 (+11.89%)</td>
</tr>
<tr>
<td>Clk WL – Tier 1 (m)</td>
<td>0.48</td>
<td>0.19 (-60.50%)</td>
</tr>
<tr>
<td>Total Clk WL (m)</td>
<td>1.03</td>
<td>0.80 (-21.67%)</td>
</tr>
<tr>
<td># Clk Buf – Tier 0</td>
<td>14,610</td>
<td>21,687 (+48.44%)</td>
</tr>
<tr>
<td># Clk Buf – Tier 1</td>
<td>12,444</td>
<td>0 (-100%)</td>
</tr>
<tr>
<td>Total # Clk Buf</td>
<td>27,054</td>
<td>21,687 (-19.84%)</td>
</tr>
</tbody>
</table>

Courtesy Panth et al., ISLPED’14
### Single Vt Power Comparisons (mW)

<table>
<thead>
<tr>
<th></th>
<th>Encounter 2D</th>
<th>Shrunken 2D</th>
<th>F2B 3D</th>
<th>F2F 3D</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Total</strong></td>
<td>618.40</td>
<td>514.40 (-16.82%)</td>
<td>522.10 (-15.57%)</td>
<td>524.00 (-15.27%)</td>
</tr>
<tr>
<td><strong>Cell</strong></td>
<td>135.60</td>
<td>126.80 (-6.49%)</td>
<td>126.10 (-7.01%)</td>
<td>126.40 (-6.78%)</td>
</tr>
<tr>
<td><strong>Net</strong></td>
<td>356.30</td>
<td>274.30 (-23.01%)</td>
<td>282.70 (-20.66%)</td>
<td>284.30 (-20.21%)</td>
</tr>
<tr>
<td><strong>Leakage</strong></td>
<td>126.50</td>
<td>113.30 (-10.43%)</td>
<td>113.30 (-10.43%)</td>
<td>113.30 (-10.43%)</td>
</tr>
<tr>
<td><strong>Memory</strong></td>
<td>49.00</td>
<td>45.10 (-7.96%)</td>
<td>45.10 (-7.96%)</td>
<td>45.00 (-8.16%)</td>
</tr>
<tr>
<td><strong>Combinational</strong></td>
<td>385.10</td>
<td>300.00 (-22.10%)</td>
<td>305.30 (-20.72%)</td>
<td>306.80 (-20.33%)</td>
</tr>
<tr>
<td><strong>Clock Tree</strong></td>
<td>62.50</td>
<td>46.90 (-24.96%)</td>
<td>48.00 (-23.20%)</td>
<td>48.50 (-22.40%)</td>
</tr>
</tbody>
</table>

Courtesy Panth et al., ISLPED’14
## Dual Vt Power Comparisons (mW)

<table>
<thead>
<tr>
<th></th>
<th>Encounter 2D</th>
<th>Shrink 2D</th>
<th>F2B 3D</th>
<th>F2F 3D</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Total</strong></td>
<td>572.10</td>
<td>471.4 (-17.60%)</td>
<td>480.10 (-16.08%)</td>
<td>482.20 (-15.71%)</td>
</tr>
<tr>
<td><strong>Cell</strong></td>
<td>131.80</td>
<td>122.5 (-7.06%)</td>
<td>123.00 (-6.68%)</td>
<td>123.30 (-6.45%)</td>
</tr>
<tr>
<td><strong>Net</strong></td>
<td>356.60</td>
<td>274.2 (-23.11%)</td>
<td>282.70 (-20.72%)</td>
<td>284.30 (-20.27%)</td>
</tr>
<tr>
<td><strong>Leakage</strong></td>
<td>83.60</td>
<td>74.7 (-10.65%)</td>
<td>74.70 (-11.00%)</td>
<td>74.60 (-10.77%)</td>
</tr>
<tr>
<td><strong>Memory</strong></td>
<td>48.80</td>
<td>45.1 (-7.58%)</td>
<td>45.10 (-7.58%)</td>
<td>45.00 (-7.79%)</td>
</tr>
<tr>
<td><strong>Combinational</strong></td>
<td>361.60</td>
<td>278.6 (-22.95%)</td>
<td>283.00 (-21.74%)</td>
<td>284.30 (-21.38%)</td>
</tr>
<tr>
<td><strong>Clock Tree</strong></td>
<td>62.50</td>
<td>47.3 (-24.32%)</td>
<td>48.00 (-23.20%)</td>
<td>48.50 (-22.40%)</td>
</tr>
</tbody>
</table>

Courtesy Panth et al., ISLPED’14
Thermal Implications of 3D ICs
Thermal Model Setup – Die, Package and Cooling Mechanism

- Compact model derived from full system cellphone model
- SoC temperature matched with full system model
Thermal Model Setup – F2B and F2F Stack up

- 3D stack-up for Face-to-Face (F2F) and Face-to-Back (F2B)
  - Back-End-Of-Line (BEOL) modeled as one layer with effective thermal properties
  - Tier 2 Silicon with vertical connections modeled as one layer with effective thermal properties
Model Generation – Power Mapping

- 2D and 3D silicon areas are similar ~ 50% area footprint shrink
- 1x1 mm² squares → 100 mm² 2D design
Model Generation – Simulation Methodology

- Influence coefficient methodology
- \[ \Delta T = \sum H_{ij} \times P_i \]
- Temperature-dependent leakage power loop
ICM Model Accuracy

- ICM based solver data compared with simulation using commercial thermal analysis tool, ICEPAK
  - Temperature delta (ICM - ICEPAK) = 0.2 °C
- Excellent match achieved between finite-volume analysis vs. ICM method

SoC Temperature distribution

(a) Our proposed model  (b) Commercial Solver

<table>
<thead>
<tr>
<th></th>
<th>ICM Max Temp (°C)</th>
<th>Commercial Solver Max Temp (°C)</th>
<th>Temp Rise Diff (°C)</th>
<th>% Temp Rise Diff</th>
</tr>
</thead>
<tbody>
<tr>
<td>SoC Temperature</td>
<td>97.0</td>
<td>96.8</td>
<td>0.2</td>
<td>0.3</td>
</tr>
</tbody>
</table>
3D Thermal Characteristics

- Power input: power distribution for a typical quad-core CPU case
- Results: Temperature difference between tiers is small < 1°C
  - Distance between tiers is very small → small thermal resistance between tiers → good mutual heating
- Power is low on each tier: ΔT = R x P

Dynamic Power Distribution

(a) 2D design
(b) Corresponding 3D design
3D Thermal Characteristics – F2B vs. F2F Integration

- Power input: power distribution for a typical quad-core CPU case
- F2F integration is slightly hotter than F2B (~ 1°C)
  - In F2F, the active layers are closer to each other
  - In F2B there is a layer of thin silicon between the two tiers which slightly helps with temperature reduction

### Dynamic Power Distribution

![Graph showing power distribution](image)

(a) 2D design  (b) Corresponding 3D design
Temperature Rise in 3D vs. 2D: IP Block Partitioning Impact

- With the same power inputs, 3D temperature is higher than 2D
- 3D temperature is very sensitive to IP block partitioning
  - Non-staggered partitioning results is higher junction temperatures, requiring 16% power reduction in 3D to match 2D
  - With only 5% power reduction in staggered partitioning, 3D temperature matches with 2D

Dynamic Power Distribution (W)  
Temperature Distribution (°C)

(a) Baseline 2D, (b) Staggered and (c) Non-staggered designs
Temperature Rise in 3D vs. 2D: Floorplanning Impact

- 3D thermal risk is lower if the high power density is placed in the center of the die
  - Temperature rise is significantly lower for center IP block (96.2°C vs. 88.8°C)
- Power saving requirement is the same for both floorplans
  - ~5% for staggered partitioning
  - ~16% for non-staggered partitioning
- Power saving is more sensitive to partitioning than floorplanning
Power Saving Opportunities in 3D

- Power savings are primarily coming from wirelength and buffer reductions
- $P_{\text{total}} = P_{\text{internal}} + P_{\text{switching}} + P_{\text{leakage}}$
- $P^{3D}_{\text{switching}} = (\alpha \cdot c_{\text{pin}} + \beta \cdot c_{\text{wire}}) \cdot P^{2D}_{\text{switching}}$
- Internal and leakage components are proportional to total cell area
Floorplanning and Partitioning Options in 3D

(a) 2D block partitioning with 2D floorplanning
(b) 2D block partitioning with 3D floorplanning
(c) 3D block partitioning with 2D floorplanning
(d) Combination of 2D and 3D block partitioning with 3D floorplanning
3D Floorplanning and Partitioning Case Study: GPU Power Intensive Case

Thermal maps of mobile MPSoC GPU intensive use-case for (a) 2D, (b) All 3D and (c) All 2D configurations
3D Floorplanning and Partitioning Case Study: CPU Power Intensive Case

![Thermal maps of mobile MPSoC CPU intensive use-case for (a) 2D, (b) All 3D, and (c) All 2D configurations](image_url)

Thermal maps of mobile MPSoC CPU intensive use-case for (a) 2D, (b) All 3D, and (c) All 2D configurations
### Summary of 3D Floorplanning and Partitioning Case Study

- 3D temperatures with appropriate partitioning / floorplanning are comparable (or even) better than 2D

<table>
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</thead>
<tbody>
<tr>
<td><strong>GPU Intensive</strong></td>
<td>2D</td>
<td>All 2D</td>
<td>63.2</td>
<td>N/A</td>
<td>0.49</td>
<td>0.85</td>
<td>2.07</td>
</tr>
<tr>
<td></td>
<td>3D (Baseline)</td>
<td>All 2D</td>
<td>64.9</td>
<td>65</td>
<td>0.21</td>
<td>0.32</td>
<td>2.11</td>
</tr>
<tr>
<td></td>
<td>3D</td>
<td>All 2D</td>
<td><strong>62.3</strong></td>
<td><strong>62.4</strong></td>
<td>0.19</td>
<td>0.28</td>
<td>1.971</td>
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Conclusions

- Practical and cost efficient 3DVLSI technologies are emerging
- A new generation of implementation tools are required to take full advantage of 3DVLSI technology
  - Floorplanner
  - Place & Route
  - Extraction
  - Timing
  - CTS
- New design methodologies are required
  - New Architectures
  - New foundation IP structures

Courtesy Saeidi et al., 3DIC’14
Thank you

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