Design Rule Management and its Applications in 15nm FreePDK Technology

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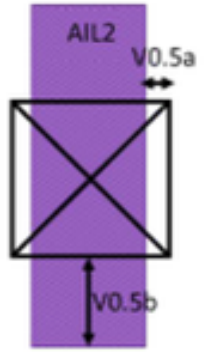
Agenda

- Traditional DRM/DRC paradigm
- Current paradigm issues
- Limitations of current method
- A new paradigm
- The iDRM system
- FreePDK15 library development using iDRM
- Rule example
- DRC deck qualification
- Conclusions

Traditional DRM/DRC paradigm

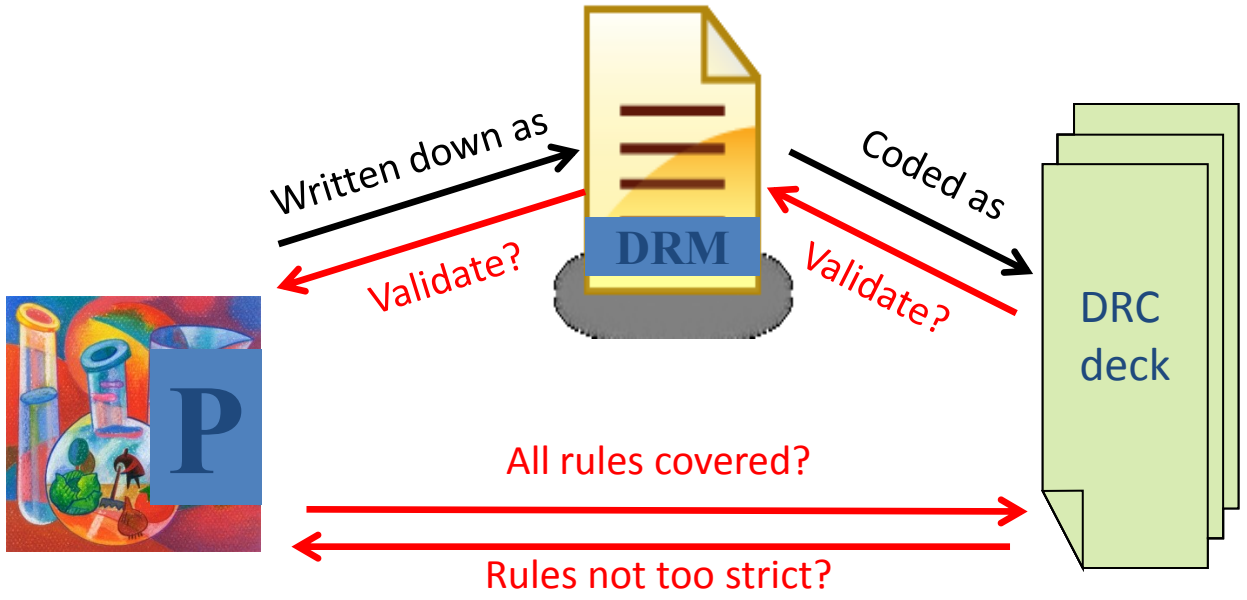
- Design rules are defined by process technology engineers
- Typically a textual description accompanied by a graphical illustration

V0.5.a	-2 nm	V0 enclosure by AIL2 on two opposite sides, horizontal direction	
V0.5.b	20 nm	V0 enclosure by AIL2 on two opposite sides, vertical direction	

- All rule descriptions and illustrations are put together in the Design Rule Manual (DRM)
- The DRM is used to develop a DRC deck

Current paradigm issues

- DRC deck takes huge effort and long time to code
  - lags behind rule definition
- No formal way to verify fidelity of DRC deck
- Decks of immature process nodes are known to have errors

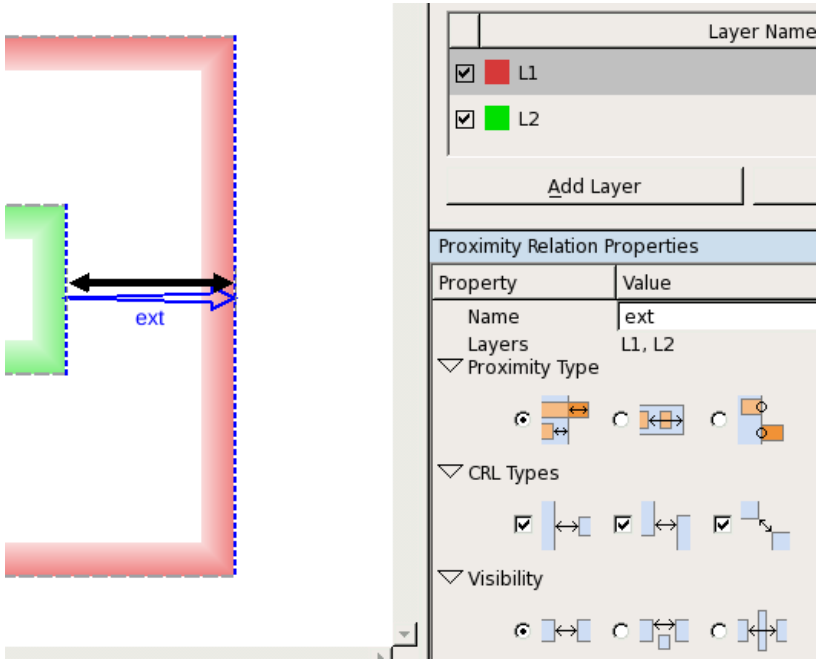


Limitations of current method

- Double work
  - Update definition, DRM
  - Update DRC deck implementation
- Consistency
  - Does the check match the rule intent?
- Update cycles
  - Two manual translation cycles, DRM update and DRC deck implementation
  - Both can introduce inconsistencies

A new paradigm

- A system that allows formal definition of design rules, that can be used for both documentation and design analysis/checks



- Enable design rule definition by non-programmers
- Rule definition should be formal, complete and unambiguous

New paradigm (2)

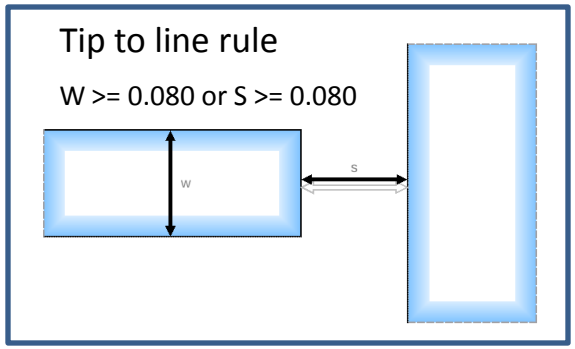
- The rule definition should be clear and …
- Executable
  - Rule definitions must be machine readable
  - Create correct-by-definition design rule checks
    - Allows interactive development of the rule by immediate checking on a layout
    - Unifies rule definition and check

The iDRM system

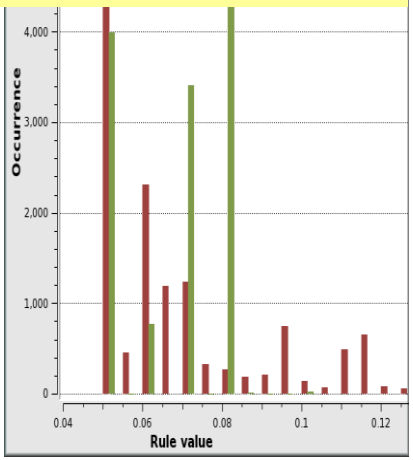
- Graphical rule entry
  - Draw the shapes (topologies)
  - Add arrows marking proximities and distances between shapes
  - Define conditions and checks
- Rules can be executed on a physical layout
  - Verify that the rule works as intended
  - Report value distribution on all found distances, in addition to pass/fail
- Rules are defined positively
  - The rule definition describes the legal condition
  - No need to program an error - an error is a violation of the legal condition

    (different concept that today's DRC checks)

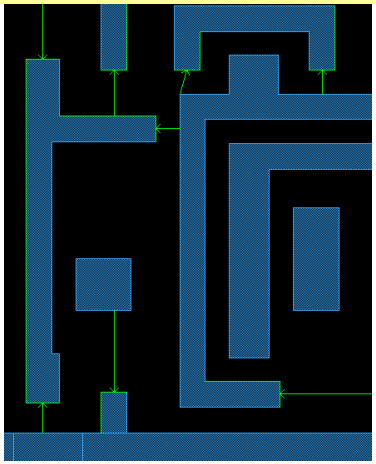
The iDRM system (2)



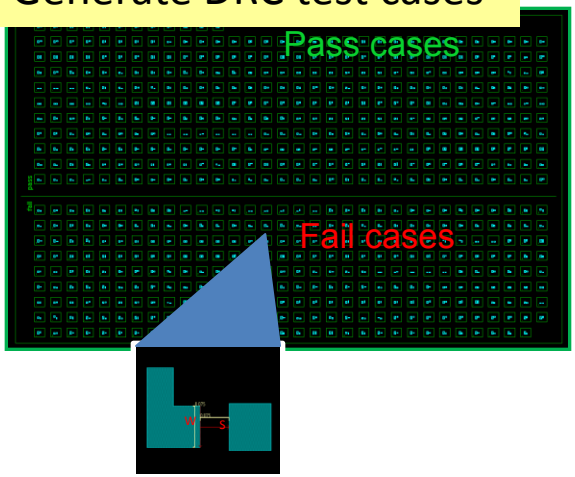
Analysis & statistics



Matches & DRC check



Generate DRC test cases

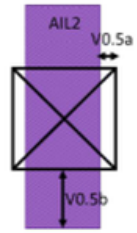


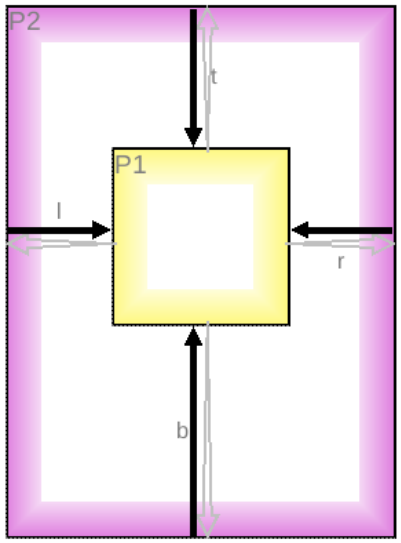
FreePDK15 library development using iDRM

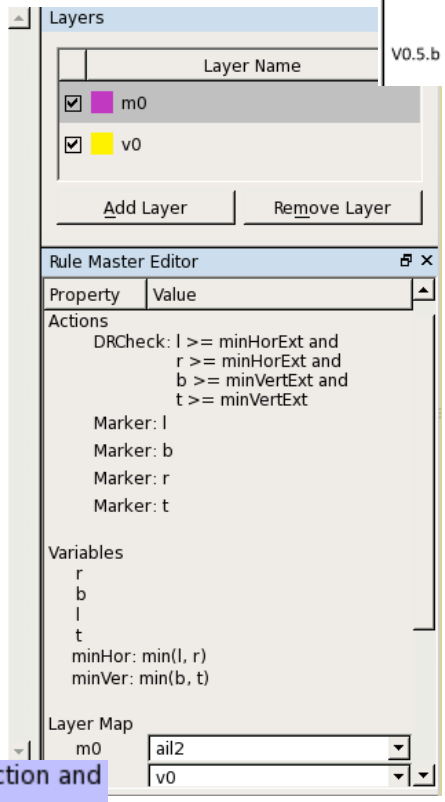
- FreePDK15 is an open source process design kit
  - Includes FinFET technology rules
  - Middle Of Line (MOL) layers
  - Cut layers
  - Double patterning layers
- We (Sage-DA) were involved in creating the standard cell library
  - Automated DRC cleanup
  - Rules were still in development and changing → DRC deck was lagging behind
  - All rules for FEOL, MOL and M1, Via1 were implemented in iDRM.
  - Additional cell architecture rules had to be defined and checked

Rule Example

- V0.5: Enclosure of V0 by AIL2

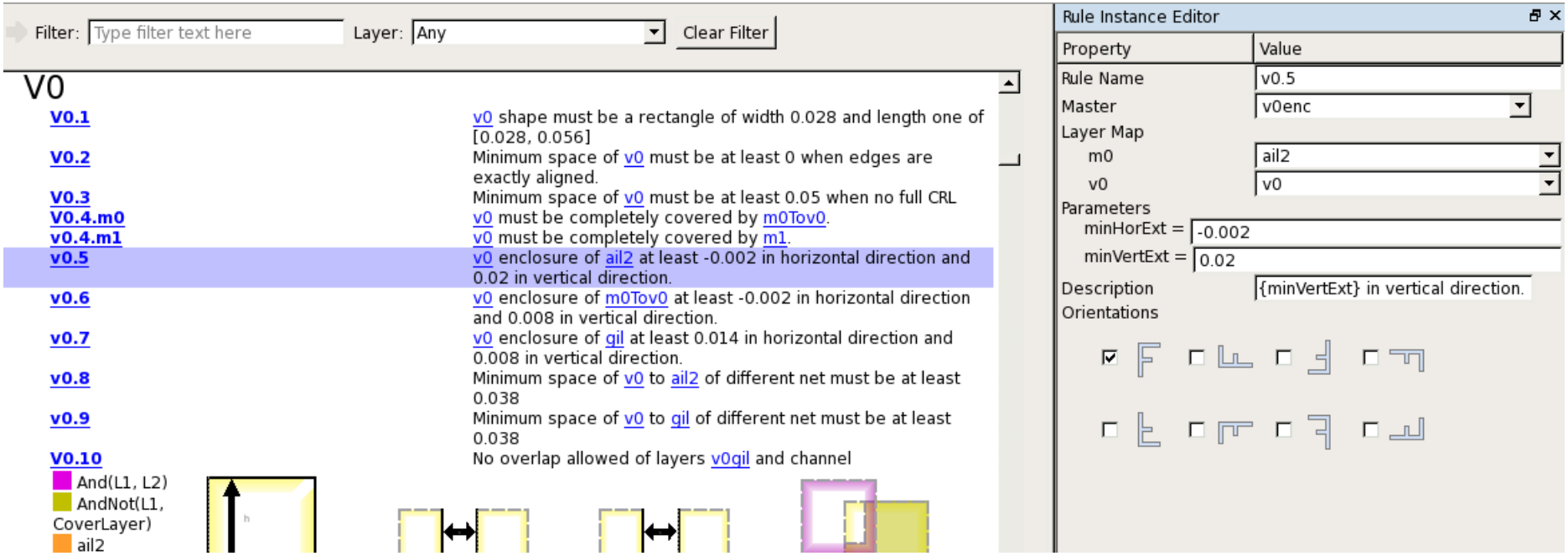
V0.5.a	-2 nm	V0 enclosure by AIL2 on two opposite sides, horizontal direction	
V0.5.b	20 nm	V0 enclosure by AIL2 on two opposite sides, vertical direction	



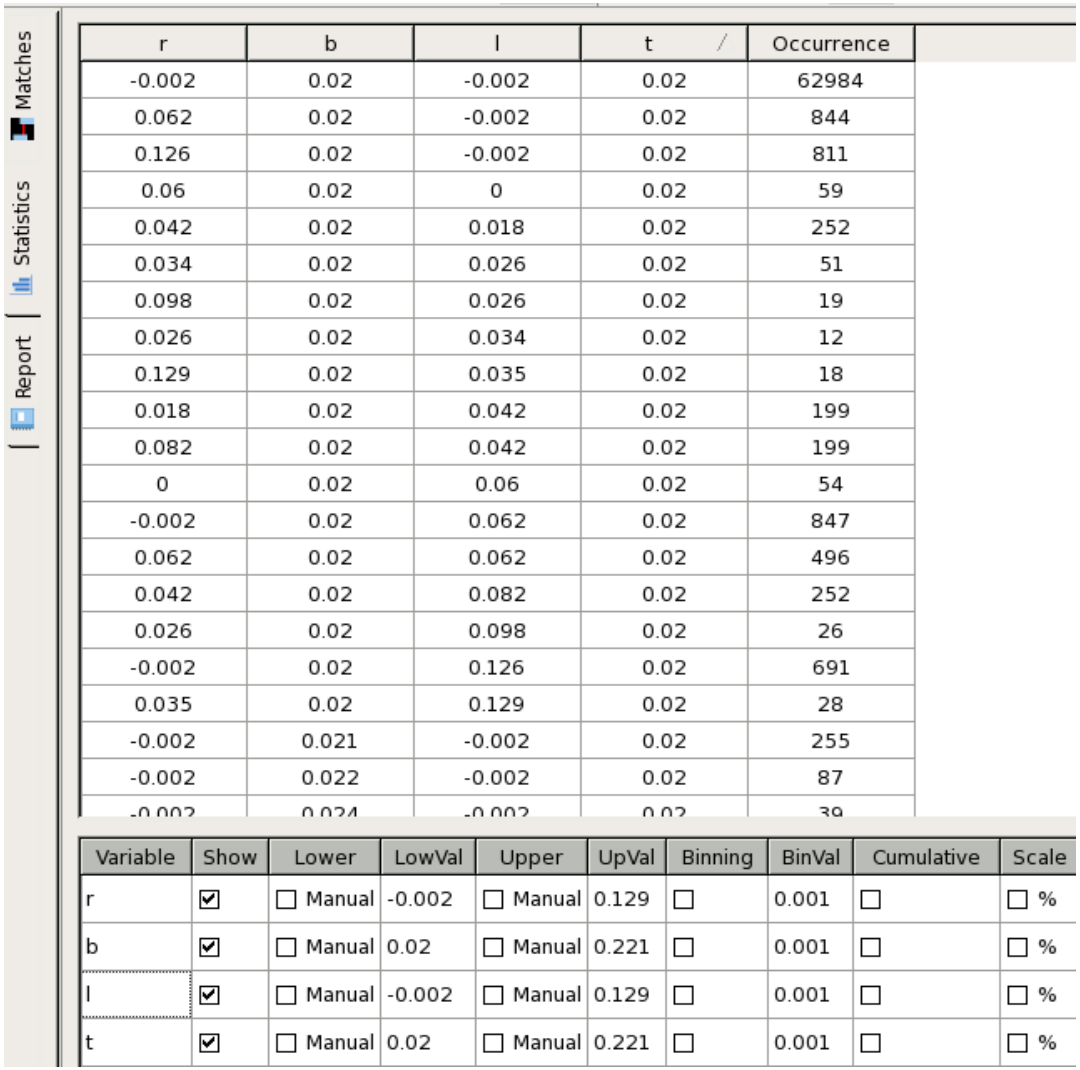


v0.5 v0 enclosure of ail2 at least -0.002 in horizontal direction and 0.02 in vertical direction.

Rule Example (2)



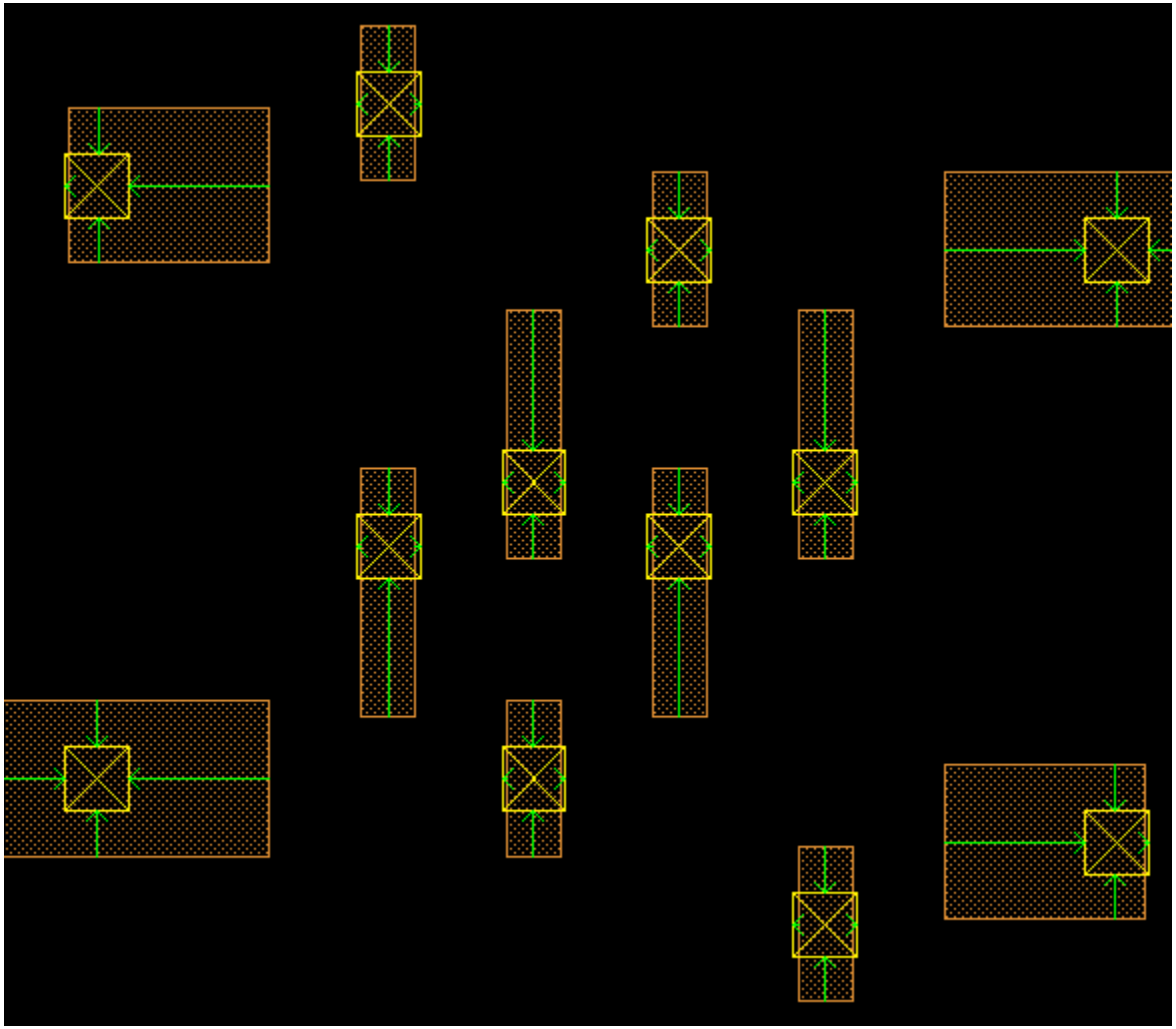
Statistical analysis



r	b	l	t	Occurrence
-0.002	0.02	-0.002	0.02	62984
0.062	0.02	-0.002	0.02	844
0.126	0.02	-0.002	0.02	811
0.06	0.02	0	0.02	59
0.042	0.02	0.018	0.02	252
0.034	0.02	0.026	0.02	51
0.098	0.02	0.026	0.02	19
0.026	0.02	0.034	0.02	12
0.129	0.02	0.035	0.02	18
0.018	0.02	0.042	0.02	199
0.082	0.02	0.042	0.02	199
0	0.02	0.06	0.02	54
-0.002	0.02	0.062	0.02	847
0.062	0.02	0.062	0.02	496
0.042	0.02	0.082	0.02	252
0.026	0.02	0.098	0.02	26
-0.002	0.02	0.126	0.02	691
0.035	0.02	0.129	0.02	28
-0.002	0.021	-0.002	0.02	255
-0.002	0.022	-0.002	0.02	87
-0.002	0.024	-0.002	0.02	39

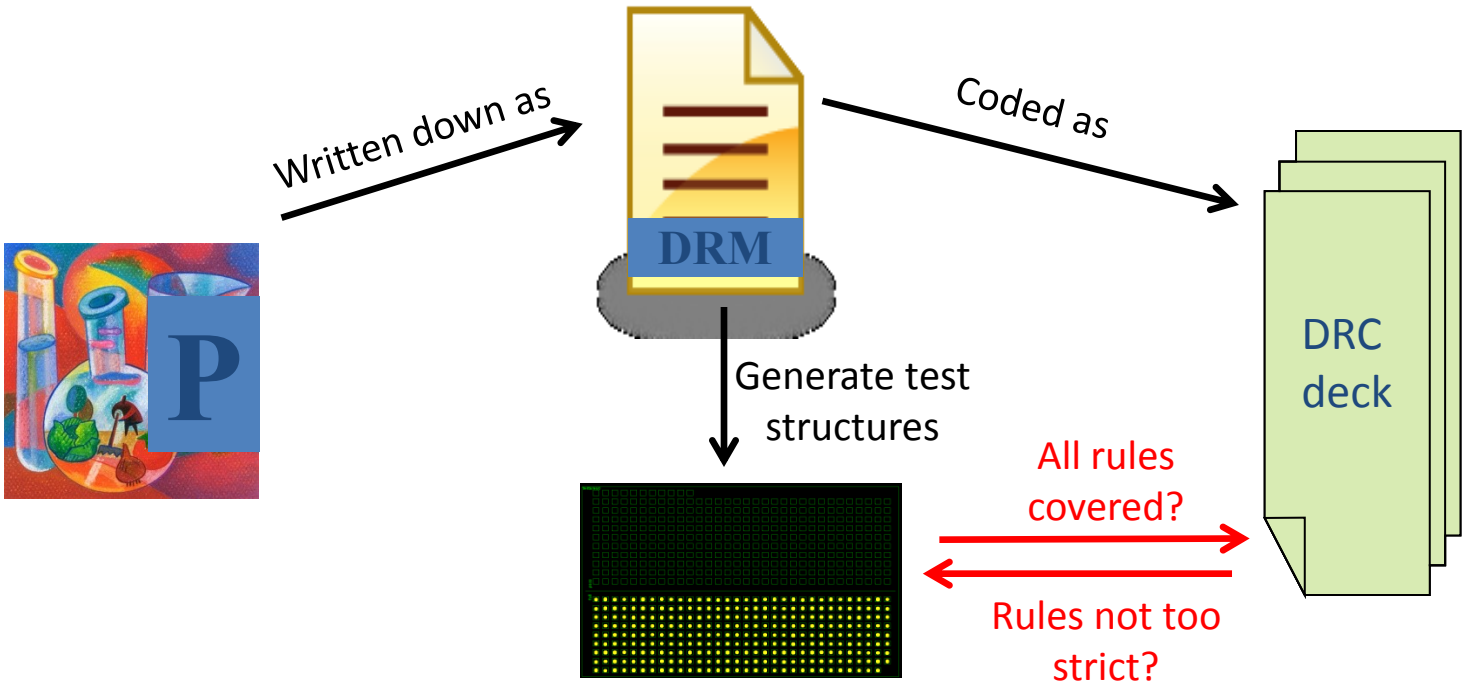
Variable	Show	Lower	LowVal	Upper	UpVal	Binning	BinVal	Cumulative	Scale
r	☑	☐ Manual	-0.002	☐ Manual	0.129	☐	0.001	☐	☐ %
b	☑	☐ Manual	0.02	☐ Manual	0.221	☐	0.001	☐	☐ %
l	☑	☐ Manual	-0.002	☐ Manual	0.129	☐	0.001	☐	☐ %
t	☑	☐ Manual	0.02	☐ Manual	0.221	☐	0.001	☐	☐ %

Rule match viewing



DRC deck qualification

- DRC deck test suite generated from same rule definition
- Used to verify third party DRC decks



Conclusions

- The current methodology for defining, documenting and creating design rules is flawed
- A single, unambiguous rule definition that is machine readable is proposed for documenting and checking rules
- The iDRM platform provides a graphical rule definition tool that is machine readable and can be immediately used for checking layout. This was used for the development of the FreePDK15 library cells
- Test structures can be generated to qualify 3rd party tool DRC deck implementations