Design Rule Management and its Applications in 15nm FreePDK Technology

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Agenda

- Traditional DRM/DRC paradigm
- Current paradigm issues
- Limitations of current method
- A new paradigm
- The iDRM system
- FreePDK15 library development using iDRM
- Rule example
- DRC deck qualification
- Conclusions
Traditional DRM/DRC paradigm

- Design rules are defined by process technology engineers
- Typically a textual description accompanied by a graphical illustration
- All rule descriptions and illustrations are put together in the Design Rule Manual (DRM)
- The DRM is used to develop a DRC deck
Current paradigm issues

- DRC deck takes huge effort and long time to code
  - lags behind rule definition
- No formal way to verify fidelity of DRC deck
- Decks of immature process nodes are known to have errors
Limitations of current method

- Double work
  - Update definition, DRM
  - Update DRC deck implementation
- Consistency
  - Does the check match the rule intent?
- Update cycles
  - Two manual translation cycles, DRM update and DRC deck implementation
  - Both can introduce inconsistencies
A new paradigm

- A system that allows formal definition of design rules, that can be used for both documentation and design analysis/checks

  - Enable design rule definition by non-programmers
  - Rule definition should be formal, complete and unambiguous
The rule definition should be clear and ...

- **Executable**
  - Rule definitions must be machine readable
  - Create correct-by-definition design rule checks
    - Allows interactive development of the rule by immediate checking on a layout
    - Unifies rule definition and check
The iDRM system

- Graphical rule entry
  - Draw the shapes (topologies)
  - Add arrows marking proximities and distances between shapes
  - Define conditions and checks
- Rules can be executed on a physical layout
  - Verify that the rule works as intended
  - Report value distribution on all found distances, in addition to pass/fail
- Rules are defined positively
  - The rule definition describes the legal condition
  - No need to program an error - an error is a violation of the legal condition (different concept that today’s DRC checks)
The iDRM system (2)

Tip to line rule
\[ W \geq 0.080 \text{ or } S \geq 0.080 \]

Analysis & statistics

Matches & DRC check

Generate DRC test cases

Pass cases

Fail cases
FreePDK15 library development using iDRM

- **FreePDK15 is an open source process design kit**
  - Includes FinFET technology rules
  - Middle Of Line (MOL) layers
  - Cut layers
  - Double patterning layers

- **We (Sage-DA) were involved in creating the standard cell library**
  - Automated DRC cleanup
  - Rules were still in development and changing → DRC deck was lagging behind
  - All rules for FEOL, MOL and M1, Via1 were implemented in iDRM.
  - Additional cell architecture rules had to be defined and checked
Rule Example

- **V0.5: Enclosure of V0 by AIL2**

  - **V0.5**
    - V0 enclosure of aii2 at least -0.002 in horizontal direction and 0.02 in vertical direction.
Rule Example (2)

**V0.1**
- v0 shape must be a rectangle of width 0.028 and length one of [0.028, 0.056]
- Minimum space of v0 must be at least 0 when edges are exactly aligned.
- Minimum space of v0 must be at least 0.05 when no full CRL
- v0 must be completely covered by m0ToV0
- v0 must be completely covered by m1

**V0.2**

**V0.3**

**V0.4.m0**

**V0.4.m1**

**V0.5**
- v0 enclosure of ail2 at least -0.002 in horizontal direction and 0.02 in vertical direction.
- v0 enclosure of m0ToV0 at least -0.002 in horizontal direction and 0.008 in vertical direction.
- v0 enclosure of ail at least 0.014 in horizontal direction and 0.008 in vertical direction.
- Minimum space of v0 to ail2 of different net must be at least 0.038
- Minimum space of v0 to ail of different net must be at least 0.038
- No overlap allowed of layers v0ail and channel

**Rule Instance Editor**

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<th>Value</th>
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<td>m0</td>
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<td></td>
<td>ail2</td>
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<td></td>
<td>v0</td>
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<td>minHorExt</td>
<td>-0.002</td>
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<tr>
<td>minVertExt</td>
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<tr>
<td>Description</td>
<td>{minVertExt} in vertical direction.</td>
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<td>Orientations</td>
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## Statistical analysis

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<th>b</th>
<th>l</th>
<th>t</th>
<th>/</th>
<th>Occurrence</th>
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| -0.002 | 0.02     | -0.002    | 0.02    | 62984
| 0.062 | 0.02     | -0.002    | 0.02    | 844
| 0.126 | 0.02     | -0.002    | 0.02    | 811
| 0.05 | 0.02     | 0       | 0.02    | 59
| 0.042 | 0.02     | 0.018    | 0.02    | 252
| 0.034 | 0.02     | 0.025    | 0.02    | 51
| 0.098 | 0.02     | 0.025    | 0.02    | 19
| 0.026 | 0.02     | 0.034    | 0.02    | 12
| 0.129 | 0.02     | 0.035    | 0.02    | 18
| 0.018 | 0.02     | 0.042    | 0.02    | 199
| 0.082 | 0.02     | 0.042    | 0.02    | 199
| 0       | 0.02     | 0.06     | 0.02    | 54
| -0.002 | 0.02     | 0.062    | 0.02    | 847
| 0.062 | 0.02     | 0.062    | 0.02    | 496
| 0.042 | 0.02     | 0.082    | 0.02    | 252
| 0.026 | 0.02     | 0.098    | 0.02    | 26
| -0.002 | 0.02     | 0.126    | 0.02    | 691
| 0.035 | 0.02     | 0.129    | 0.02    | 28
| -0.002 | 0.021    | -0.002   | 0.02    | 255
| -0.002 | 0.022    | -0.002   | 0.02    | 87
| -0.002 | 0.027    | -0.002   | 0.02    | 58

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<th>Upper</th>
<th>UpVal</th>
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</table>
DRC deck qualification

- DRC deck test suite generated from same rule definition
- Used to verify third party DRC decks

Diagram:
- DRM
  - Written down as
  - Coded as
  - Generate test structures
  - All rules covered?
  - Rules not too strict?
Conclusions

- The current methodology for defining, documenting and creating design rules is flawed.
- A single, unambiguous rule definition that is machine readable is proposed for documenting and checking rules.
- The iDRM platform provides a graphical rule definition tool that is machine readable and can be immediately used for checking layout. This was used for the development of the FreePDK15 library cells.
- Test structures can be generated to qualify 3rd party tool DRC deck implementations.