Load-Aware Redundant Via Insertion for Electromigration Avoidance

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Outline

Load-Aware Redundant Via Insertion for Electromigration Avoidance

- Electromigration Avoidance
- Redundant Via Insertion
- Load-Awareness
- Implementation: Flow
- Results: Benchmark

Summary
Electromigration

- Dependencies:
  - Current density
  - Interconnect geometry
  - Temperature
  - Material
  - Manufacturing process

Electromigration: Outlook

- Future shrinking of IC structures [ITRS]

- Increase of resistance
  - Incomplete AC self healing

\[ J = \frac{I}{A} \]
\[ I/I_{\text{ref}} \]
\[ A/A_{\text{ref}} \]

Electromigration (EM) and Stress Migration (SM)

- Atom migration due to EM and SM

- Divergence of total atom migration

Redundant Via Insertion: Principle

- Vias are prone to IC failure

- Inserting redundant vias

  - Reliability
  - Chip yield
  - Resources

Redundant Via Insertion: Process

Optimization algorithm for insertion solution ("as many as possible")
Redundant Via Insertion: Problem

- Layout example
  - One redundant via location
  - Qualifies for segment 1 and 2
    - Redundant via in segment 1 or 2?
- “EM-aware Redundant Via Insertion” [Pak, 2015]
  - $J \Rightarrow V_{\text{void}} \Rightarrow T_{\text{failure}}$
  - if $T_{\text{failure}} > T_{\text{lifetime}}$ then $EM_{\text{stable}}$ else $EM_{\text{critical}}$

No consideration of:
- Current density*
- Segment length
- Time-dependent stress

*within $EM_{\text{critical}}$ or $EM_{\text{stable}}$
Load-Awareness: Influence of $j$, $l$ and $\sigma(t)$

- Current density ... $j$, stress ... $\sigma(t)$
  - $j \Rightarrow \text{EM}(j)$
  - $\sigma \Rightarrow \text{SM}(\sigma)$
  - $t_{\text{depletion}} \Rightarrow \sigma(t_i) = \sigma_{\text{crit}} \Rightarrow \text{void}$
  - $\sigma_{\text{max}} \geq \sigma_{\text{crit}} \Rightarrow \text{EM critical}$
  - $\sigma_{\text{max}} < \sigma_{\text{crit}} \Rightarrow \text{EM stable}$

- Segment length ... $l$
  - $jl \Rightarrow \sigma_{\text{max}}$

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Load-Awareness: Example

- **Current density:**

  - EM stable
  - EM critical

- **Segment length:**

  \[ j \ell_{\text{seg}_1} \ll j \ell_{\text{seg}_2} \]
Load-Awareness: Example

- Current density:

- Segment length:

  - EM critical

\[ j l_{seg1} = = j l_{seg2} \]

\[ t_{seg1} \ll t_{seg2} \]
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Summary
Implementation: Flow

Read Technology and Design Information

Acquire Input Capacity and Output Current

Propagate Currents in Net Graph

Search for Redundant Via Locations

Build Conflict Graph w. Inner and Outer Edges

Calculate Weights in Conflict Graph

Redundant Via Insertion

Electromigration Avoidance

Load-Awareness

Flow

Results

Calculate Weights in Conflict Graph: Basics

- **Segment load**
  - $j, l$ and $\sigma(t)$

- **Metric: load per via = vertex weight ($w$)**

\[
w_i = \frac{\text{seg. load}_{\text{max}}}{\#\text{via}^*} \Rightarrow w_i = \left(\frac{t_{\text{min}}}{t_i} + \frac{(JL)_i}{(JL)_{\text{max}}}\right) \frac{n_i}{\sigma_{\text{crit}}} \Rightarrow t_i = \begin{cases} 
\infty & \text{if } \sigma_{\text{max}} < \sigma_{\text{crit}} \text{ (EM stable)} \\
t_{i, \text{crit}} & \text{if } \sigma_{\text{max}} > \sigma_{\text{crit}} \text{ (EM critical)} 
\end{cases}
\]

*to connect two segments

---

Calculate Weights in Conflict Graph: Details

- Redundant vias:

  Weights consider:
  - Interconnect bending ($l\uparrow$)
  - Number of vias ($1/n$)
  - On/off track vias ($l\uparrow$)

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Set Up Constraints and Solve 0-1 ILP Problem

Load-Awareness

Electromigration Avoidance

Redundant Via Insertion

Flow

Results

Set Up Constraints and Solve 0-1 ILP Problem

Minimize:
\[ z = \sum_{i \in V} \infty w_i v_i \quad v_i \in \{0,1\} \]

- Inner edges:
\[ \sum_{j \in IE} \infty v_j = 1 \]

- Outer edges:
\[ v_i + v_j \leq 1, \quad i, j \in OE \]

Speed-up technique: divide into small problems [Lee et al., 2008]

- Pre-selection of vertices with minimum weight and no outer edges

Electromigration Avoidance
Redundant Via Insertion
Load-Awareness
Flow
Results

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EM-Robust Via Configurations

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Summary
Results

- **Reduction in:**
  - Total,
  - Average, and
  - Maximum via load,
  
  compared to results of via insertion by Chen [5].

- **Verification:**
  - Reduction in average and peak via stress

<table>
<thead>
<tr>
<th>Name</th>
<th>Design [5]</th>
<th>Our design</th>
<th>Total via load</th>
<th>Total</th>
<th>Average</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>mcc1</td>
<td>1147.1</td>
<td>1050.8</td>
<td>8.4</td>
<td>4.1</td>
<td>31.1</td>
<td></td>
</tr>
<tr>
<td>mcc2</td>
<td>6710.7</td>
<td>5978.7</td>
<td>10.9</td>
<td>5.2</td>
<td>4.5</td>
<td></td>
</tr>
<tr>
<td>primary1</td>
<td>44</td>
<td>128</td>
<td>8.1</td>
<td>5.3</td>
<td>28.2</td>
<td></td>
</tr>
<tr>
<td>primary2</td>
<td>55</td>
<td>1168.1</td>
<td>5.5</td>
<td>11.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>s5378</td>
<td>2383.7</td>
<td>2192.6</td>
<td>8.0</td>
<td>5.5</td>
<td>9.9</td>
<td></td>
</tr>
<tr>
<td>s9234</td>
<td>2958.7</td>
<td>2703.5</td>
<td>8.6</td>
<td>5.8</td>
<td>9.9</td>
<td></td>
</tr>
<tr>
<td>s13207</td>
<td>90</td>
<td>590.2</td>
<td>1.4</td>
<td>1.1</td>
<td>0.2</td>
<td></td>
</tr>
<tr>
<td>s15850</td>
<td>1271.1</td>
<td>1168.1</td>
<td>8.1</td>
<td>5.3</td>
<td>28.2</td>
<td></td>
</tr>
<tr>
<td>s38417</td>
<td>2958.7</td>
<td>2703.5</td>
<td>8.6</td>
<td>5.8</td>
<td>9.9</td>
<td></td>
</tr>
<tr>
<td>s38584</td>
<td>90</td>
<td>590.2</td>
<td>1.4</td>
<td>1.1</td>
<td>0.2</td>
<td></td>
</tr>
<tr>
<td>struct</td>
<td>6710.7</td>
<td>5978.7</td>
<td>10.9</td>
<td>5.2</td>
<td>4.5</td>
<td></td>
</tr>
</tbody>
</table>

Summary

- **Electromigration Avoidance**: Required in future
- **Redundant Via Insertion**: Opportunity
- **Load-Awareness**: $j, l$ and $\sigma(t)$

- Implementation: Flow
- Results: Reduction in total, average and maximum via load

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Added intelligence into redundant via insertion to avoid EM

- Easy add-on with significant reliability increase