Generalized Force Directed Relaxation with Optimal Regions and Its Applications to Circuit Placement: A Tribute to Professor Satoshi Goto

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An Efficient Algorithm for the Two-Dimensional Placement Problem in Electrical Circuit Layout

SATOSHI GOTO, MEMBER, IEEE

Abstract—This paper deals with the optimum placement of modules on a two-dimensional board, which minimizes the total routing length of signal paths. A new heuristic procedure, based on iterative improvement, is proposed. The procedure repeats random generation of an initial solution and its improvement by a sequence of local transformations. The best among the local optimum solutions is taken as a final solution. The iterative improvement method proposed here is different from the previous one, in the sense that it considers interchanging more than two modules at the same time and examines only a small portion of feasible solutions which has high probability of being better. Experimental results show this procedure gives better solutions than the best one up to now. The computation time for each local optimum solution grows almost linearly with regard to the number of modules.

Satoshi Goto (M'77) was born in Hiroshima, Japan, on January 3, 1945. He received the B.E. and M.E. degrees in electronics engineering from Waseda University, Tokyo, Japan, in 1968 and 1970, respectively, and the Ph.D. degree in engineering from Waseda University in 1977, for his research on computer-aided network design, graph theory, and combinatorial optimization methods.

He joined Nippon Electric Company in 1970 and is now a Supervisor of the Application System Research Laboratory, Central Research Laboratories. He has been engaged in the research and development of computer application system for LSI layout design, traffic control system and transmission or communication network design. He is now in charge of developing an advanced interactive CAD system for custom LSI and PWB. During 1975–1976 he was on leave at the Electronics Research Laboratories, University of California, Berkeley, where he worked on LSI layout and large-scale network design problems.

Dr. Goto is a member of the Institute of Electronics and Communication Engineers of Japan and the Operation Research Society of Japan.
Outline

Placement Basics

Prof. Goto’s 1981 Milestone Work

Applications to Modern Placement

Future Research Directions
Circuit Placement

- Place objects into a die s.t. no objects overlap with each other & some cost metric (e.g., wirelength) is optimized

842K cells
646 macros
868K nets

12,752 cells
247 macros
$A_{\text{max}}/A_{\text{min}} = 8416$

wirings among modules (cells/macros) are not shown here!!
Placement Algorithm Paradigms

- **Constructive algorithm**: Places a module at a desired position and fix its position.
  - Cluster growth, min cut, QP, etc.

- **Iterative algorithm**: Modifies a placement to improve its solution quality until some termination condition is met.
  - Force-directed method, nonlinear placement, etc

- **Nondeterministic approach**: Applies a probabilistic model to determine the placement process
  - Simulated annealing, genetic algorithm, etc.

Initial solution → Improvement → refinement

could combine multiple elements
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**SORG**
**constructive initial placement**
- Sub-Optimal Random Generation (SORG)
- Sequentially selects unplaced modules based on their connectivity to other modules and places them in their **optimal regions** to minimize the total wirelength.

**GFDR**
**iterative improvement**
- Goto Force-Directed Relaxation (GFDR)
- Repeatedly interchanges a set of modules in optimal or near-optimal regions to minimize the total wirelength.
Optimal Region [Goto 1981]

- **Objective**: \( \min \left( \sum_{i=1}^{6} |x_1 - \tilde{x}_{1,i}| + \sum_{i=1}^{6} |y_1 - \tilde{y}_{1,i}| \right) \)

- Module \( m \)'s **optimal region** is formed by the medians of the boundaries of its net bounding boxes (excluding \( m \))
Optimal Region [Goto 1981]

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[FastPlace, NTUplace]
**Goto Force-Directed Relaxation** [Goto 1981]

- Repeatedly interchanges modules to minimize wirelength
- Compute the optimal region for a module, fixing all others

- \(\epsilon\)-neighbor(\(m\)): Modules with the Manhattan distance \(\leq \epsilon\) to module \(m\)'s optimal location
- For a module \(m\), GFDR computes \(m\)'s \(\epsilon\)-neighbors; for each \(m\)'s \(\epsilon\)-neighbor, GFDR further computes its \(\epsilon\)-neighbors, etc. until \(\lambda\) modules are identified
- Select the \(\lambda\) module exchange sequence with the minimum total wirelength, if any.

![Diagram with modules and connections]

1-neighbor, 3-exchange sequence:

\[
A \rightarrow B \rightarrow G \rightarrow A \\
A \rightarrow B \rightarrow K \rightarrow A, \text{ etc.}
\]
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Typical Modern Circuit Placement Flow

- Global Placement (GP)
  - Computes the best position for each module to minimize the cost (e.g., wirelength), ignoring module overlaps
- Legalization (LG)
  - Places modules into row and removes all overlaps among modules
- Detailed Placement (DP)
  - Refines the solution

Chen, et al., “A high quality analytical placer considering preplaced blocks and density constraint,” ICCAD-06 (TCAD-08)
Placement with Density Constraint

- Given a chip region and module dimensions, divide the placement region into bins
- Determine \((x, y)\) for all movable modules

\[
\begin{align*}
\min & \quad W(x, y) \quad \text{// wirelength function} \\
\text{s.t.} & \quad 1. \text{Density}_b(x, y) \leq \text{MaximumDensity}_b \\
& \quad \text{for each bin } b \\
& \quad 2. \text{No overlap between modules}
\end{align*}
\]
Multilevel Global Placement

Cluster the modules based on connectivity/size to reduce the problem size.

Iteratively decluster the clusters and further refine the placement.

Initial placement

clustering

clustered module

....... chip boundary
mPL: GFDR for Multilevel Refinement [ICCAD-05]

- Chan et al., “Multilevel optimization for large-scale circuit placement,” ICCAD-05
- For a module, extended GFDR computes its $\epsilon$-neighbors and randomly selects one to further compute the new $\epsilon$-neighbors, until $\lambda$ modules are identified
- Extended GFDR tries all module permutations in the sequence to find the best placement
- Six 3-exchange sequence:
  no exchange, $A \leftrightarrow B$, $A \leftrightarrow G$, $B \leftrightarrow G$, $A \rightarrow B \rightarrow G \rightarrow A$, $A \rightarrow G \rightarrow B \rightarrow A$.  

All six 3-exchange sequences are explored
Different VT cells can be fabricated by controlling the dopant concentration during ion implantation.

A low or high VT cell may violate the minimum implant area (MIA) constraint if its PMOS or NMOS implant area is too small.

If cell height is uniform: MIA constraint → minimum cell width constraint.

Minimum Implant Area (MIA) Constraint

- Implant area > MIA constraint
- Implant area < MIA constraint

Violations

OK
Cell Abutting for Solving MIA Constraints

- Could insert fillers to cells to make a bigger implant area
- Abutting violating cells of the same VT could lead to smaller area overhead than filler insertion alone

![Diagram showing initial placement, violating cells, filler insertion, and cell abutting processes.]

- Bigger area!!
- Smaller area!!
- Cell abutting
- Filler insertion
- Swap $c_3$ with $c_5$
- Shift $c_3$ and $c_6$
NTUplace: MIA-Aware Placement [DAC-16]

- Transform an MIA-violating placement to a cluster-based placement and solve it by traditional placement methods.
**Optimal Region (OR) Based Clustering**

- Cluster violating cells of the same VT in their ORs
  - Minimize wirelength while satisfying the MIA constraint
- OR for a cell: \( \min \left( \sum_{i=1}^{6} |x_1 - \tilde{x}_{1,i}| + \sum_{i=1}^{6} |y_1 - \tilde{y}_{1,i}| \right) \)
- OR for a 2-cell cluster with \( m_i \) nets connecting to cell \( c_i \):
  \[
  \min \left( \sum_{i=1}^{2m_1} |x_1 - \tilde{x}_{1,i}| + \sum_{i=1}^{2m_1} |y_1 - \tilde{y}_{1,i}| + \sum_{i=1}^{2m_2} |x_2 - \tilde{x}_{2,i}| + \sum_{i=1}^{2m_2} |y_2 - \tilde{y}_{2,i}| \right)
  \]
Partial Layouts (2.5%): Ours vs. Baseline

- Circuit: mgc_pci_bridge32_1
- MIA: 10 site steps; LVT: 10%, HVT: 10%
- Area: 14.5% smaller
- Wirelength: 30.4% shorter

Area overhead!!
FastPlace/POLAR: [ISPD-05/ICCAD-13]


- Fixing all other modules, an unlocked module can be moved to its optimal region if the target bin has enough unlocked modules to balance density.

![Diagram showing module movement chains]

Original module position and move chains

Two move chains

New module position after movement
Outline

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Applications to Modern Placement

Future Research Directions
Future Placement Challenges

Scalability

Multi-dimension

Heterogeneity

Technology
Modern Placement Challenges

- High complexity
  - Tens of millions of modules to be placed

- Placement constraints
  - Preplaced modules
  - Chip density, etc.

- Mixed-size placement
  - Hundreds/thousands of large macros with millions of small standard cells

- Many more
  - 3D IC
  - Analog, etc.

10M+ placeable modules
mixed-size design

1000+ macros
SoC design

3D IC

FinFET

[EE Times'04]
Multi-Cell-Height Placement

- Mixed-cell-height cells complicate placement, due to cell heterogeneity and power-rail alignment
  - Higher cells provide greater drive strengths at the cost of larger areas and power.
- Need new formulations for the computations of ORs, force directed relaxation, bin selection from \( \epsilon \)-neighbors, esp. with additional design constraints (minimum implant area, etc.)

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A B C D

VDD
VSS
VDD
VSS
VDD
Mixed-Size Placement

- Pre-designed macros might preserve metal layers for interior routing, incurring routing blockages
- Need to consider macro positions and orientations for accurate OR and $\epsilon$-neighbor computations
  - More complex for multi-domain mixed-size designs and additional constraints (region/fence constraints, etc.)
Routability/Timing-Driven Placement

- The original OR and $\varepsilon$-neighborhood formulations are for wirelength optimization
- Need to develop routabilty/timing-driven OR and force-directed relaxation formulations
  - New net weight models?

Wirelength-driven

Routability-driven
FinFET-Based Placement

- Self-heating is a key constraint to FinFET-based design
- Design challenges: Quantized transistors and number of fingers, self-heating effect (SHE) aware placement
- Fin-to-fin heating is more dominating than device-to-device heating, and central region in a device is hotter
- Need to consider the special properties for OR, $\epsilon$-neighborhood, and GDFR computations

3-fin FinFET

heat profile: TSMC’s simulation

gate

width direction

strong effect

weak effect

fin

length direction
FPGA Placement

- Keys issue in modern FPGA architectures: **heterogeneous logic components, segmented routing structures**
- Need to consider the special architectures for OR and GDFR computations

Segmented wiring (HPWL is not accurate!!)
Thermal-aware 3D IC Placement

- Through-silicon vias (TSVs) cause significant challenges for 3D IC placement
- Need to reserve whitespace for TSV insertion and consider 3D structures for OR, $\epsilon$-neighborhood, and GDFR computations
Conclusions

- Prof. Goto’s 1981 milestone work has reshaped the landscape of modern placement
  - FastPlace, mPL, NTUplace, POLAR, etc.
- Placement challenges: scalability, multi-dimension, heterogeneity, technology
- Could extend the OR, $\epsilon$-neighborhood, and GDFR formulations to handle emerging challenges
Thank You!

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