Challenges and Opportunities in Automotive, Industrial, and IOT Physical Design

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Introduction

Keynotes

Background

Outcome

Outline

- **Market Drivers**
- **Technology Evolution**
- **Design Method Evolution**
- **Physical Design Directions**

Outline

Market Drivers

Technology Evolution

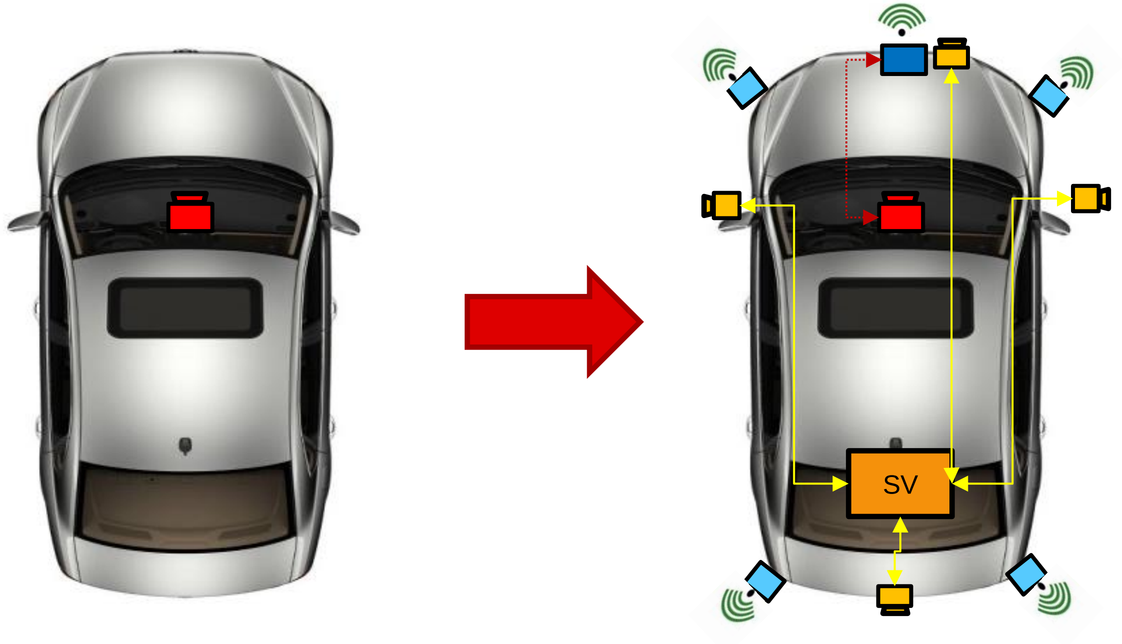
Design Method Evolution

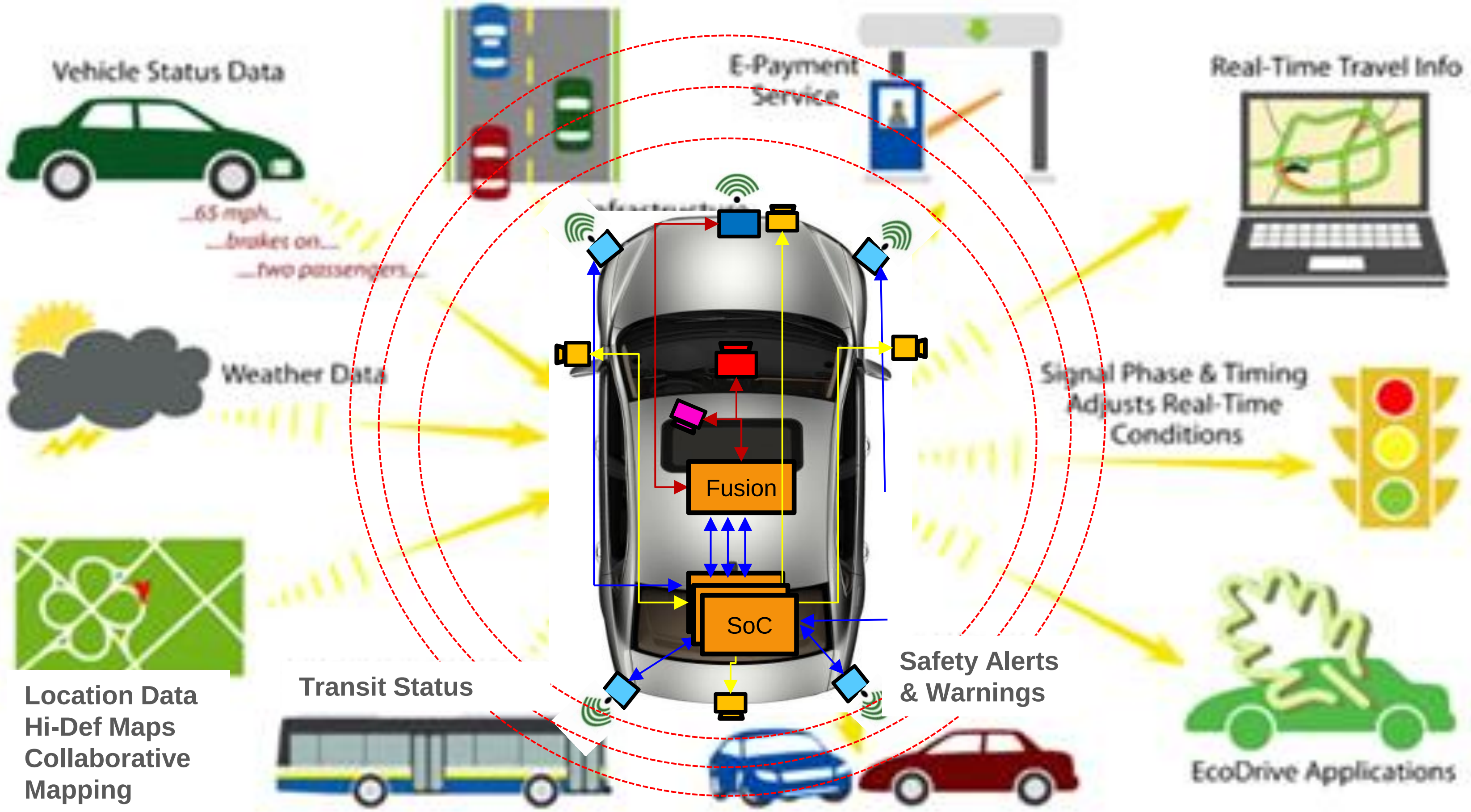
Physical Design Directions

Automotive Markets

Few sensors

More sensors





Passive Assist to Limited Driver Substitution

- Isolated compute provides security
- Few sensors per SoC with some limited fusion
- Simple classification moving to Deep Learning

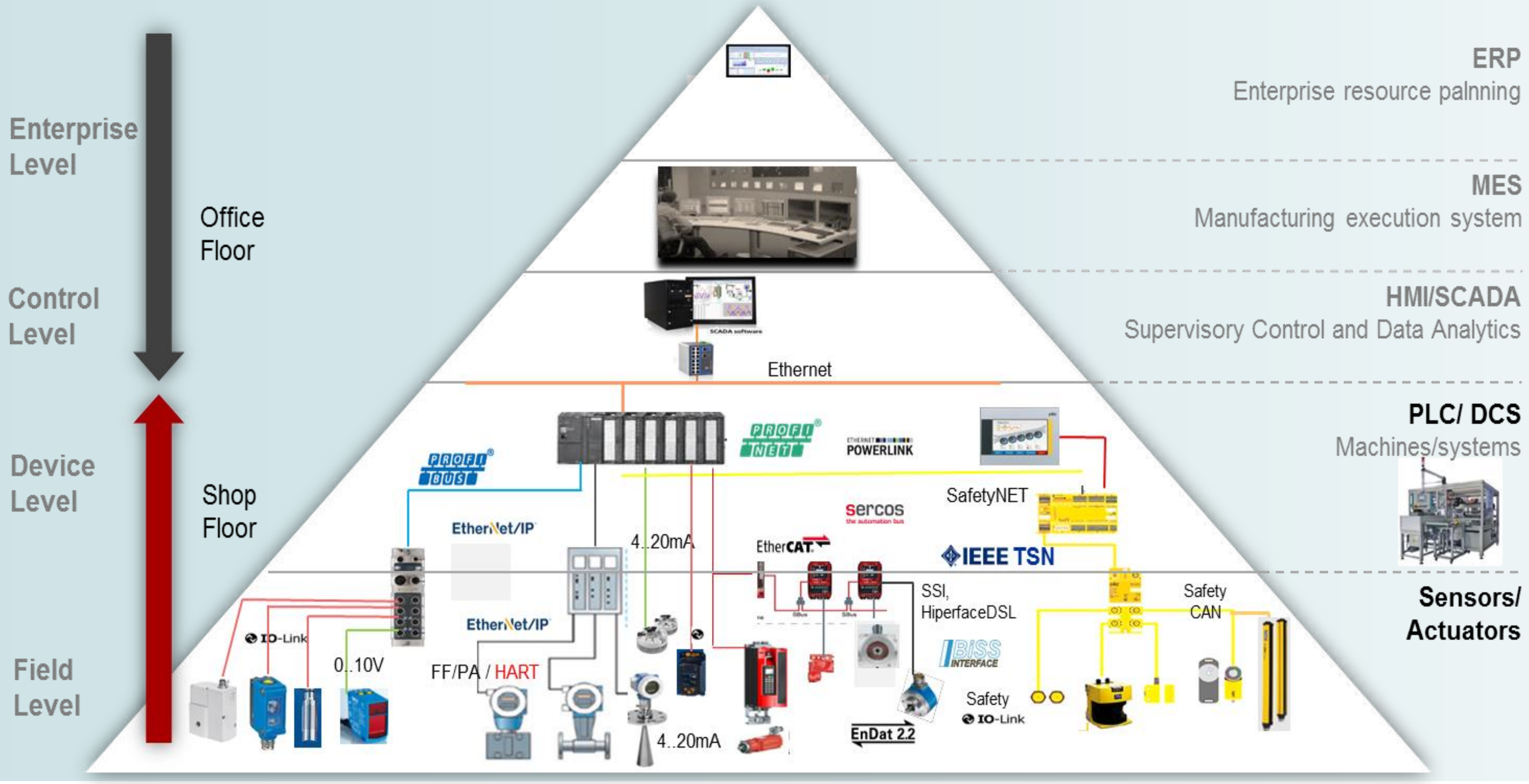
Autonomous Driving with Connected Technology

- Connected compute needs active security
- Multi-Modal Sensor Fusion provides Robustness and Redundancy
- Heavy use of Deep Learning

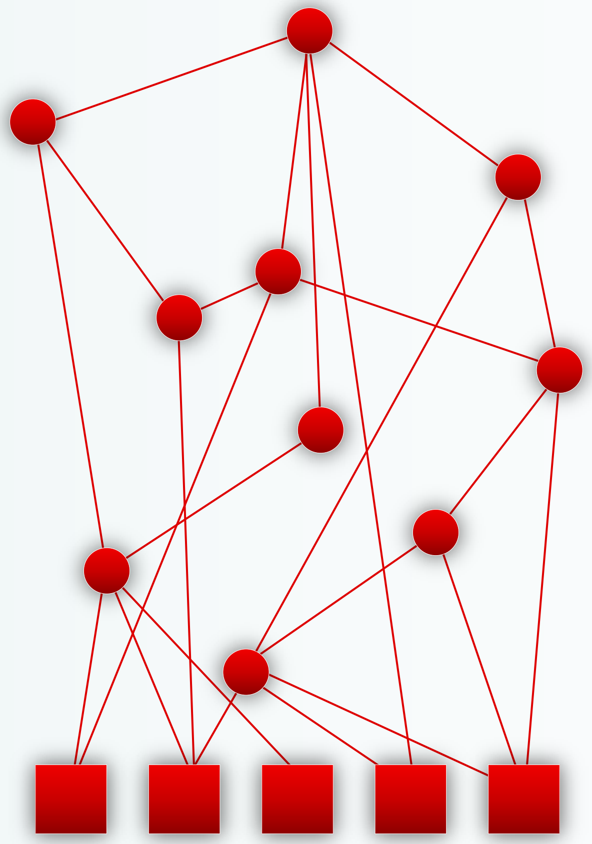
ADAS → **Autonomous**

Industrial Applications

Multi Layer Architecture

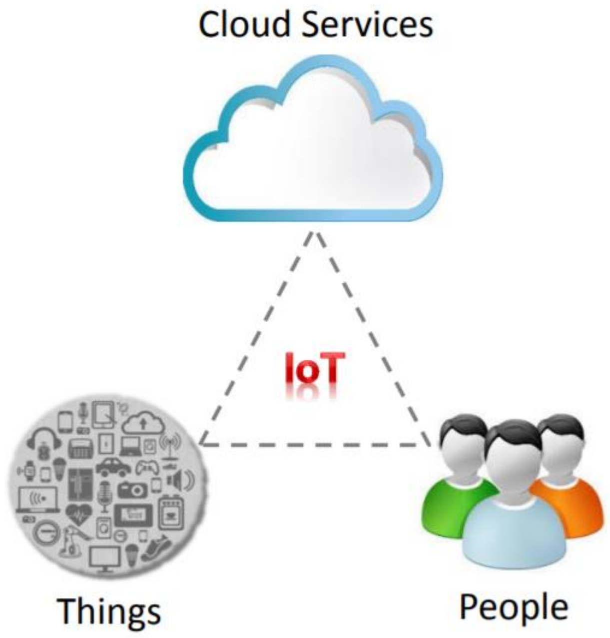


Cyber-physical system (CPS) based automation



Today → **Future**

IOT Overview



Wearables
- Entertainment
- Fitness

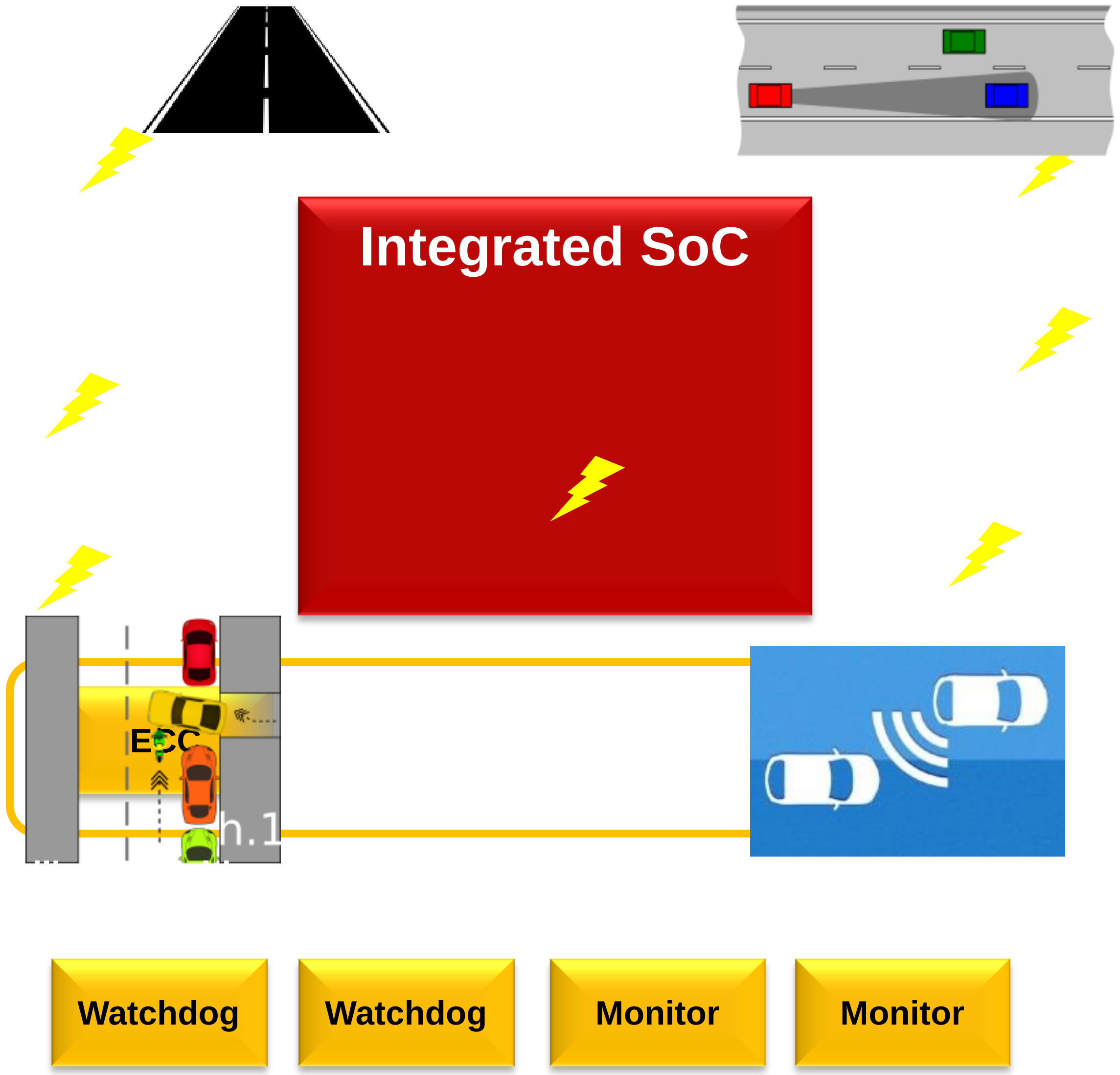
Automation
- Access Control
- Light and Temp

Smart Cities
- Residential E-meters
- Smart Street lights

Manufacturing
- Flow Optimization
- Real-time inventory

Health Care
- Remove Monitoring
- Asset tracking

Safety for Automotive, Industrial, and IOT



- Integration has driven more potential **system** faults inside the SOC.
- We must address these with redundant or fail-safe solutions.
- Physical Design plays a critical roll.

Summary: Market Challenges

- Reliability
  - Producing long-lived products with low failure rates.
- System Integration
  - Board-level issues now present in SOC-level design.
- Adaptability
  - Markets moving faster than SOC design cycle times.
- Ubiquity
  - More sockets; more applications; lower power and distributed applications.

Outline

- Market Drivers
- **Technology Evolution**
- Design Method Evolution
- Physical Design Directions

(Obligatory Technology Scaling Slide)

Classic Dennard Scaling

TABLE I

Scaling Results for Circuit Performance

Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox}, L, W	$1/\kappa$
Doping concentration N_a	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance $\epsilon A/t$	$1/\kappa$
Delay time/circuit VC/I	$1/\kappa$
Power dissipation/circuit VI	$1/\kappa^2$
Power density VI/A	1

Dennard, et al. Journal Solid State Circuits, Oct. 1974.

- Faster
- Cheaper
- Lower Power

The Rise of Variation

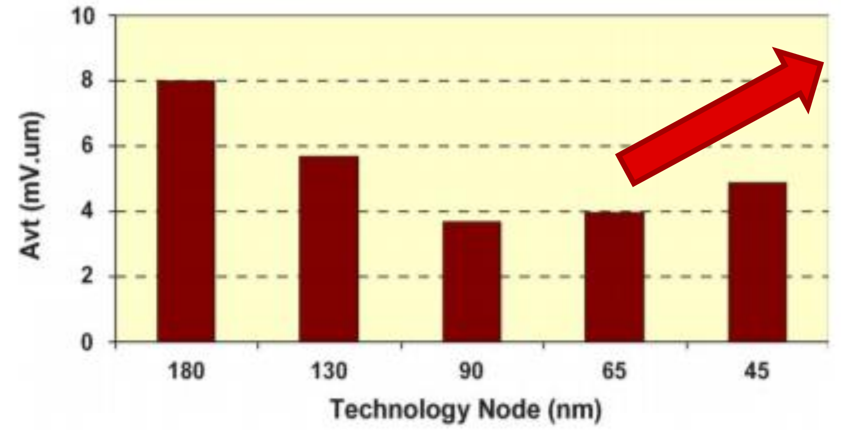
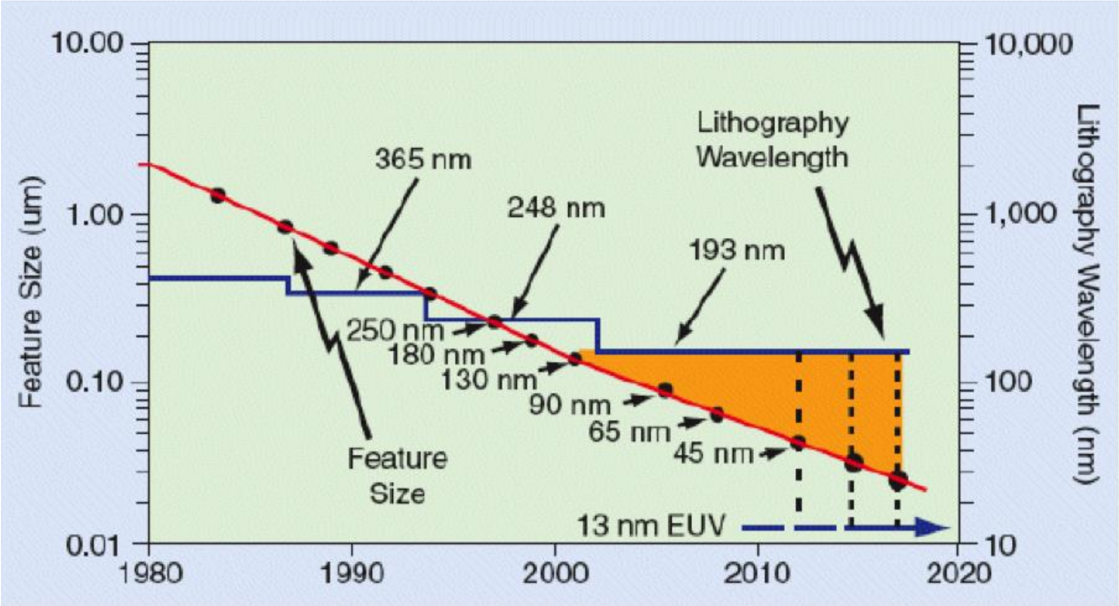


Fig. 16. NMOS local mismatch trend over multiple generations.

Saxena, et al. IEEE Trans. On Electron Devices, Vol 44, No1, p 131.

- More Complex

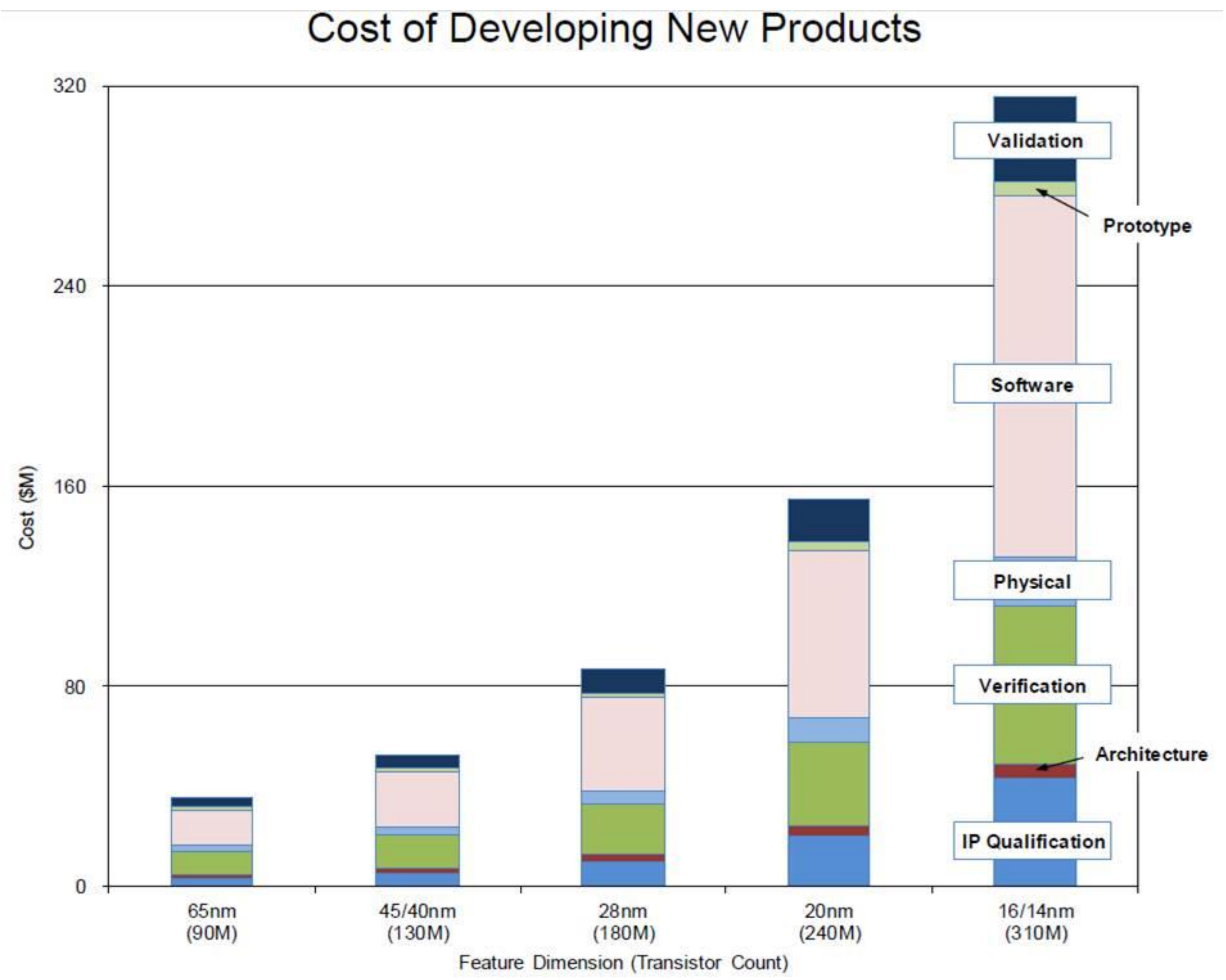
Lithographic Complexity



S. Borkar, “Design challenges for gigascale integration,” presented at the 37th IEEE/ACM Int. Symp. Microarchitecture, Portland, OR, 2004.

- Not cheaper
- Possibly not faster
- Lower power per operation
- (Much) More Complex

Cost Trends



Source: IBS, http://semiengineering.com/how-much-will-that-chip-cost/

- Large-scale integration
  - Multi-core, multi-architecture devices.
- True ‘system on a chip’ designs
  - Analog and complex IP integration.
- Increasing development cost.
  - First-pass silicon ‘success’
  - Emergence of ecosystem solutions

Summary: Technology Challenges

- Complexity
  - Technology-driven complexity and system complexity.
- Variability
  - Uncertainty in design and complexity in design signoff.
- Cost
  - Design cost optimization to build viable products.
- Ecosystem
  - Analog and dissimilar IP integration

Outline

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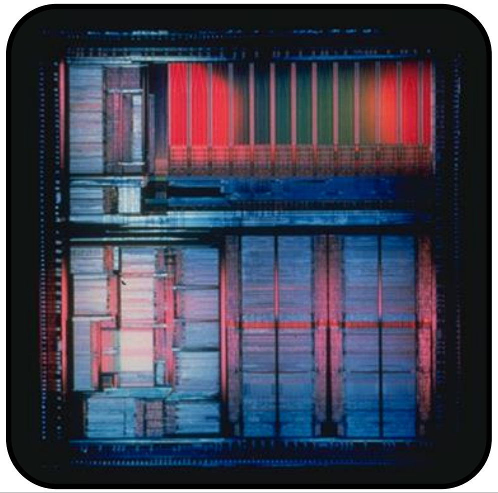
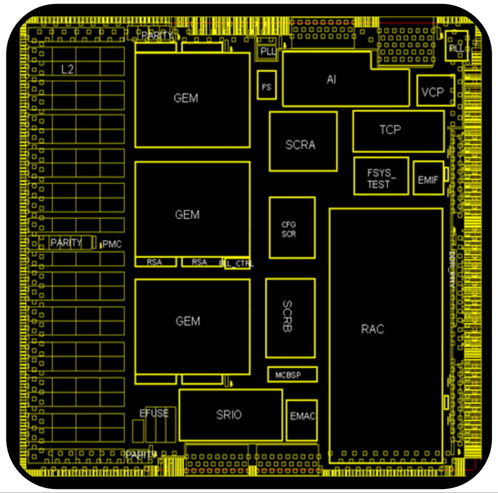
Design Evolution

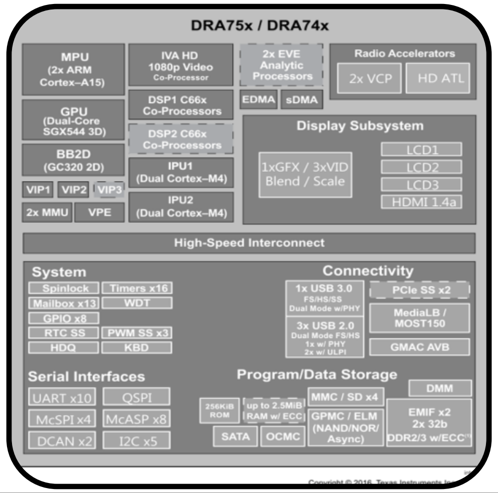
~1995



~2006

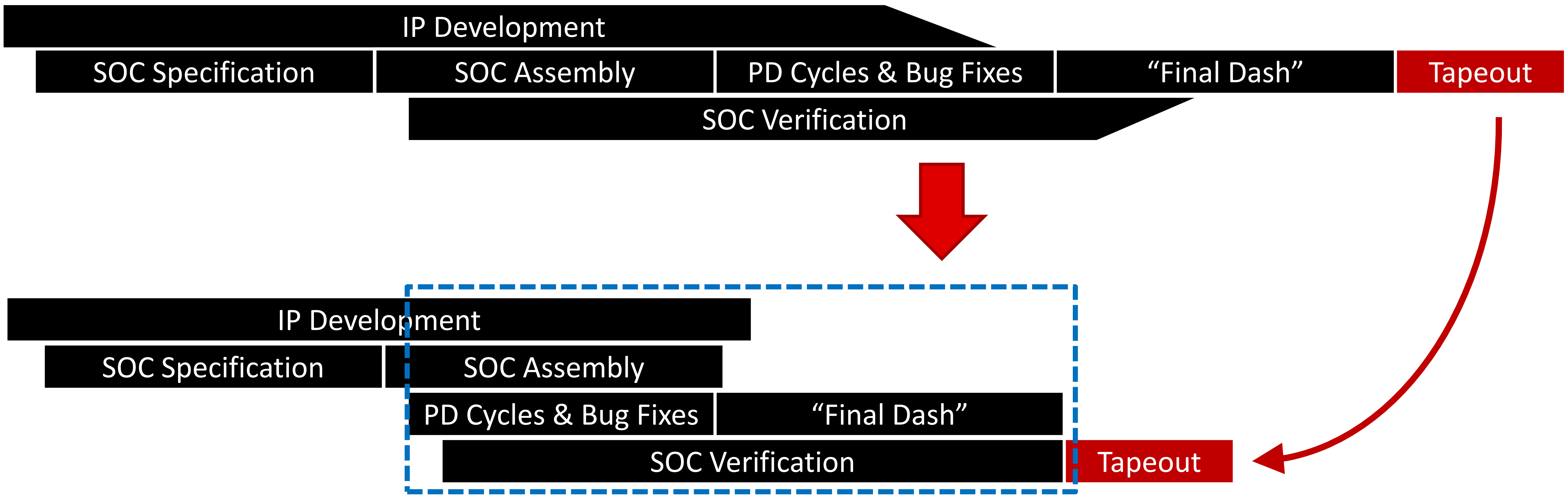


~2018



~1995	~2006	~2018
Custom Process	Custom ➔ Foundry Process	Foundry Process
Custom IP	Custom ➔ Ecosystem IP	Ecosystem IP
Internal EDA	Ecosystem EDA	Ecosystem/Foundry EDA
100k➔1M objects	10➔100M+ objects	100M’s➔B+ objects
Hand + Auto Synthesis + P&R	Mostly Auto Synthesis + P&R	(Physical) Synthesis + P&R
Cap-based Simple STA	Manual ECO/Timing Closure	Auto ECO/Timing Closure
Simple “MHz” GPIO	SI-based STA	Variation-aware STA
	DDR, ~5GHz SERDES	Analog, PM, DDR, SERDES, …

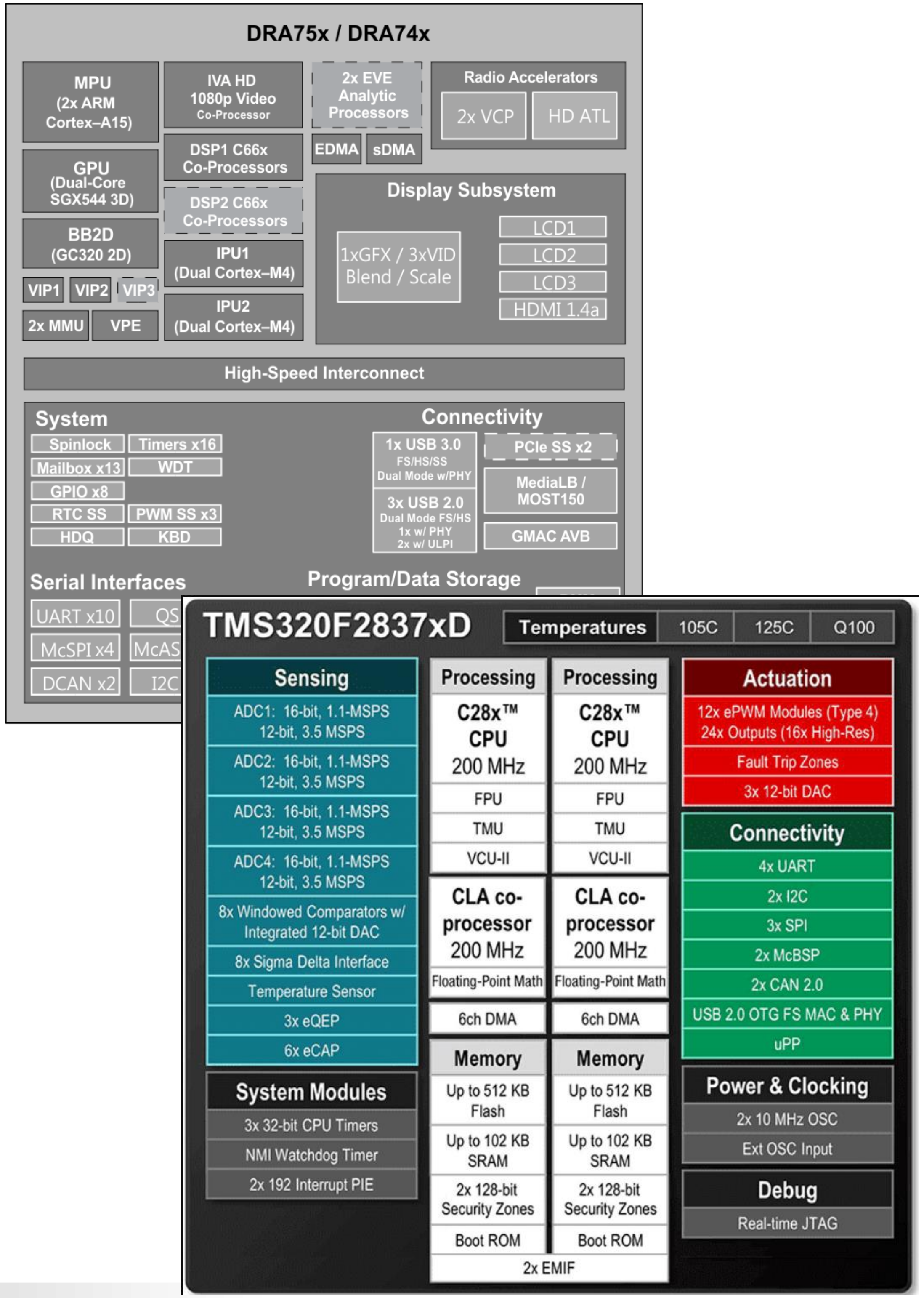
Cycle Time Compression



- Physical Design overlap with IP development, SOC assembly, and verification.
- New challenge introduced with dirty data and more iterative design.

SOC Evolution

- Highly-Integrated Systems (especially IOT)
- Complex Clocking & Systems
  - Generally driven by external interfaces, low-power communication standards, etc.
  - Example: 200k instance IOT design, 200 source clocks, average 12 clocks / register, 1200 total clock domains
- Re-use
  - Investment costs drive need to re-use macros across multiple devices in a node.
- Non-Traditional Advanced Node Adoption
  - Driven by lower power, ease-of-use, flash integration, etc.



Summary: Design Methods

- Cycle Time
  - Overlapping PD with other domains.
- Constraints
  - Complex constraints and dissimilar IP interactions.
- Integration
  - Analog IP integration with unique requirements.
- Advanced Nodes
  - Wider adoption creating QOR, TAT, and ease-of-use challenges.

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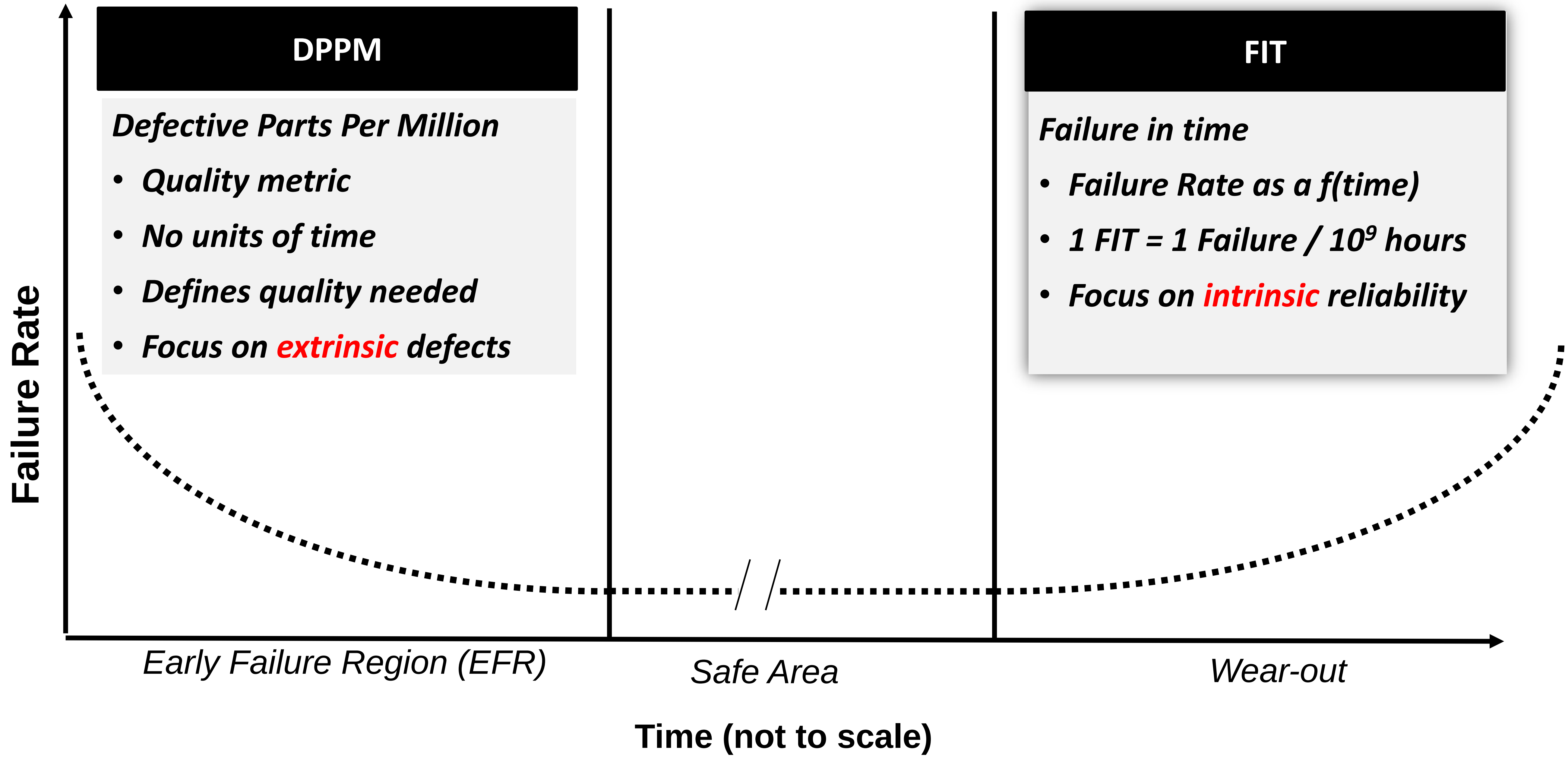
- **Physical Design Directions**

Reliability

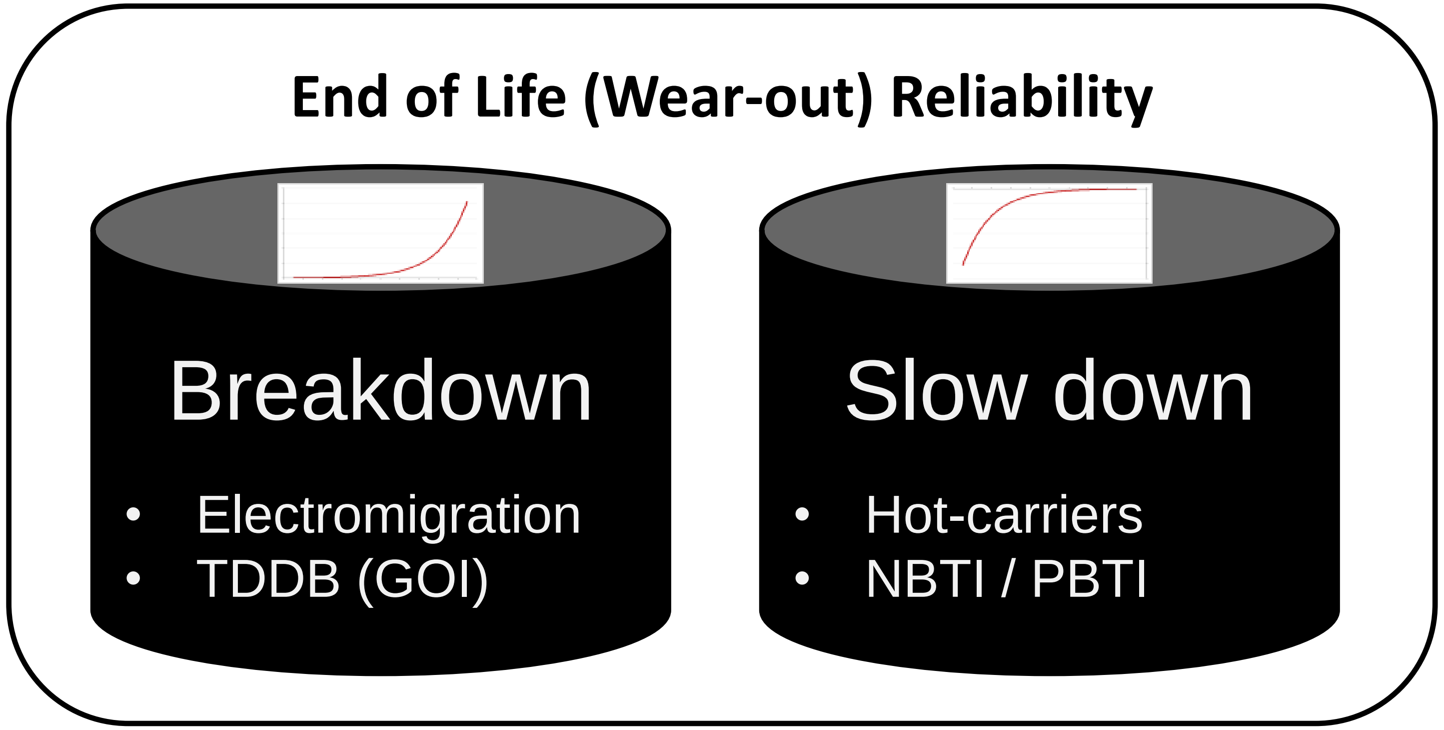
Key Metrics for Quality and Reliability



Intrinsic Reliability Market Requirements

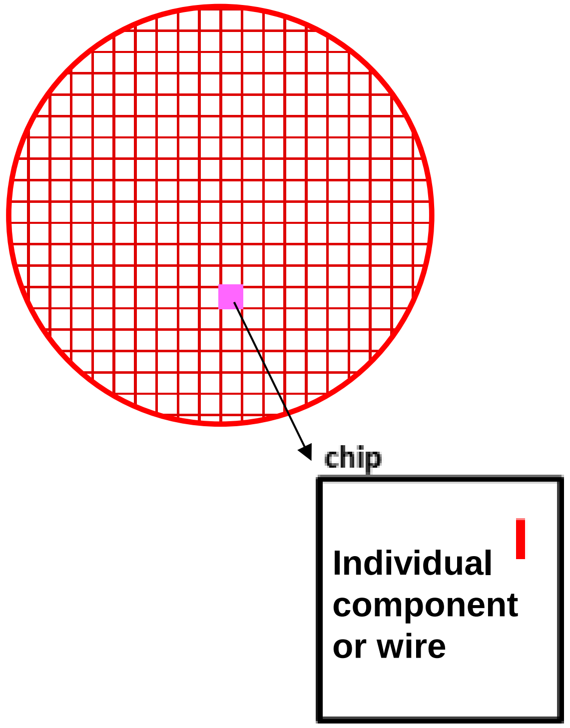
	Consumer	Infrastructure	Industrial	Infotainment	Safety
Life	3-5 Years	10 Years	10 - 20 Years	10-15 Years	10-20 Years
Tj	90C	105C	125C+	125C	125C+
POH	<100K	100K	100-200K	12.5 to 20K	12.5-100+K
FIT	50	<50	1-5	1-5	0.1-2
ECC	Minimal	Critical RAMs	~ All RAMs	Critical RAMs	All RAMs

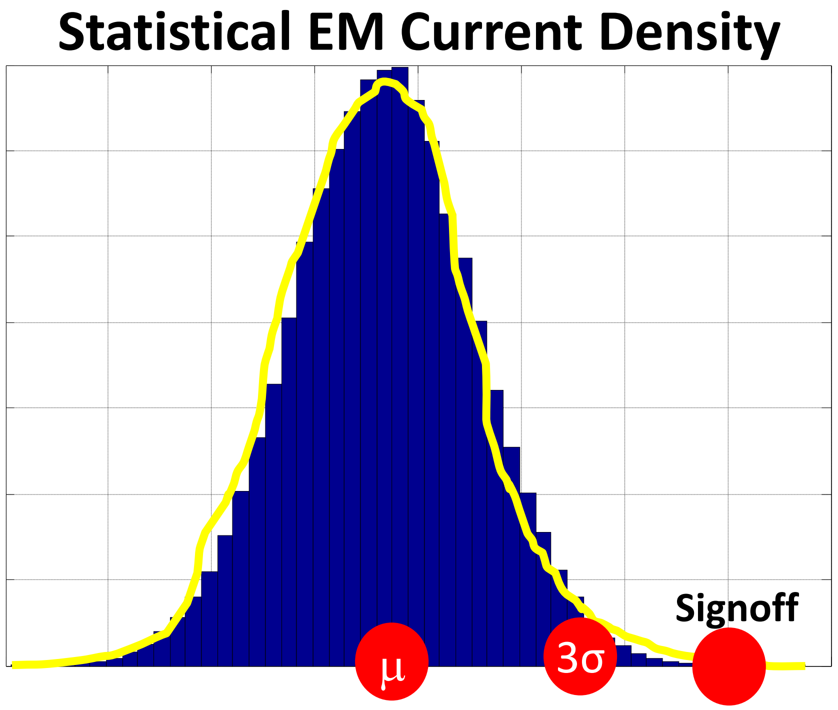
Tighter FIT requirements constrain designs.



Temperature extremes challenge reliability closure.

Measuring Reliability



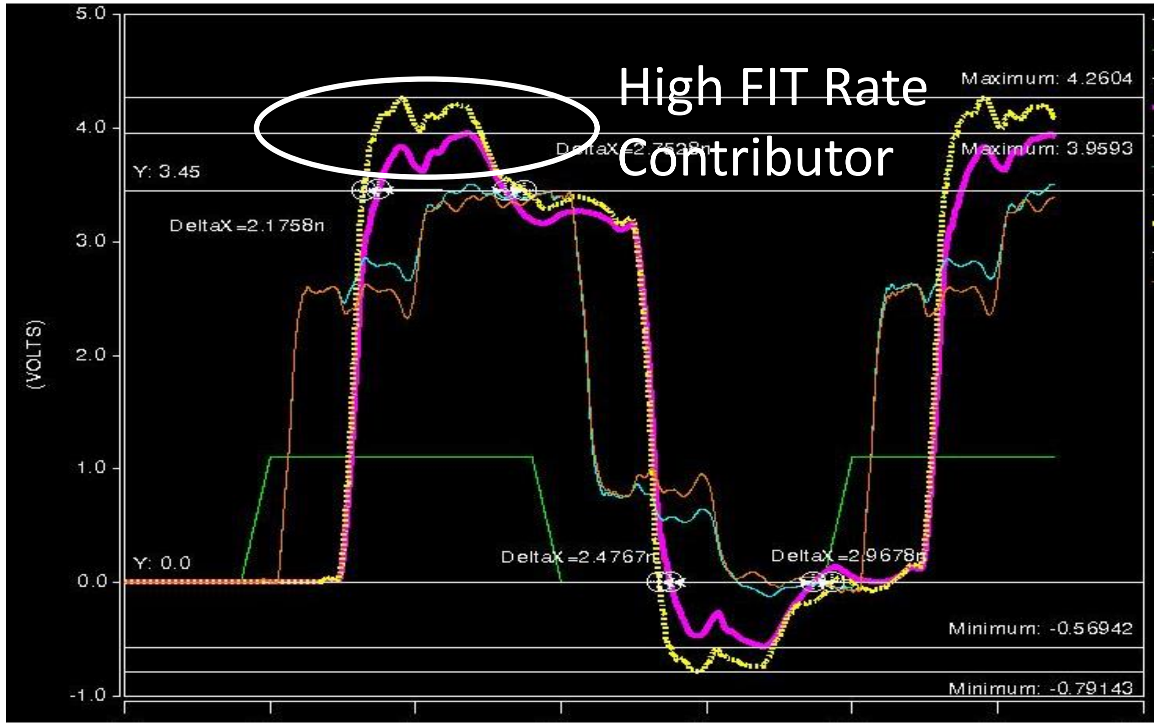


Consumer and Infrastructure

- Simple, conservative signoff methodologies
- Conservative signoff to specs.
- Hard to quantify margin

Industrial, Infotainment, Safety

- Requires early reliability budgeting
- Typically complex calculators and simulation
- Conservative signoff to specs
- FIT estimation models: f(process, environment, etc.)
- Calculators for scaling across various use conditions



Self Heating

- Self and Local Heating
  - FinFETs have limited paths for thermal conductivity.
  - Local heating can slow or cause device failure.
  - Self-Heating exacerbates long-term EM/HCI/BTI
- Metal system now has three design concerns
  1. Power delivery
  2. Signal transmission
  3. **Heat transport**
- Physical Design Impact
  - Placement of local heat" generators" and impact on critical paths.
  - Sizing and buffering to reduce localized heating
    - E.g., more buffers on non-critical signals to minimize local heating.

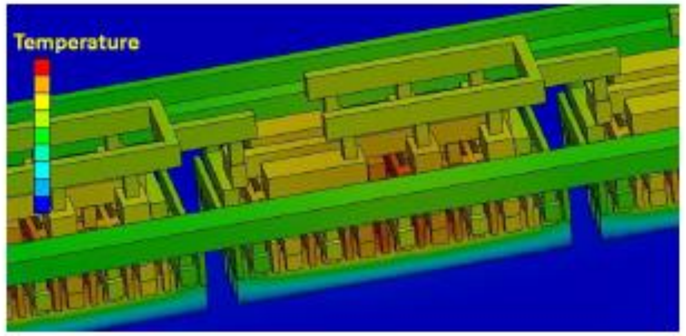


Fig. 11 The temperature profile of a ring oscillator is studied by FEM in this study.

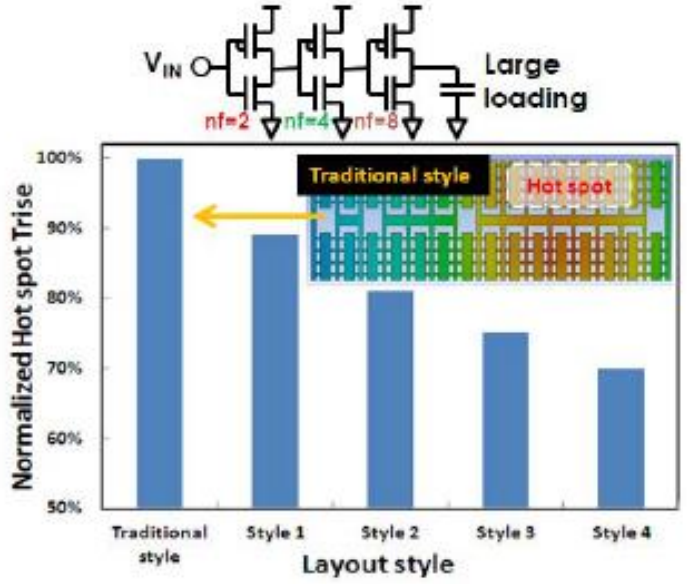


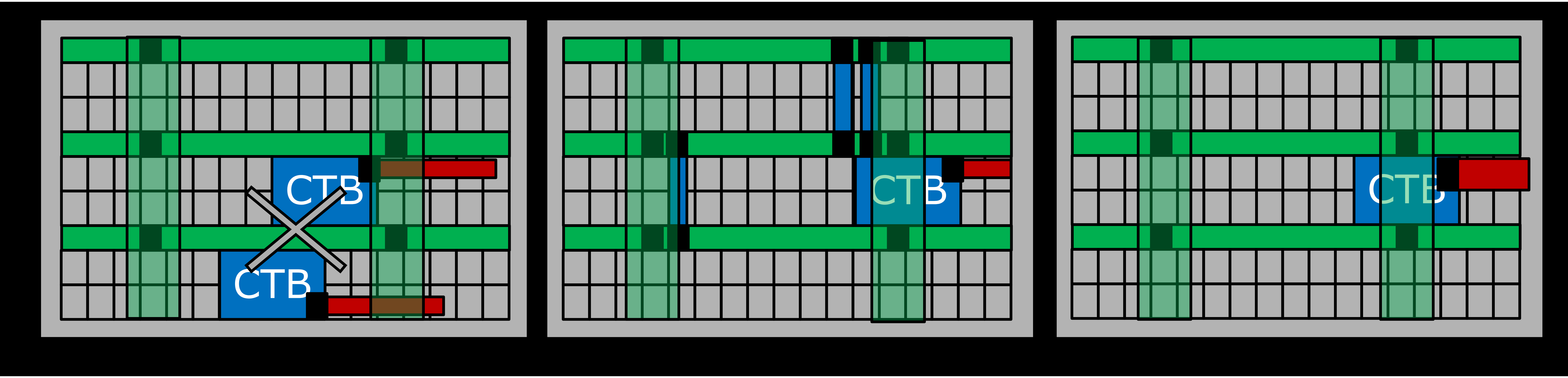
Fig 12. Simulated temperature rise from different layout styles of an inverter buffer chain. The circuit schematic, input signal and loading are exactly the same for all layout styles.

Thermal Behavior of Self-heating Effect in FinFET Devices Acting on Back-end Interconnects C.W. Chang eta. al. 2015

Opportunities in Reliability Estimation

- Reliability Calculators
    - Ability to scale across use conditions and consider variation.
- Reliability Budgeting
    - Framework for early budgeting; IP ecosystem aware.
- Reliability Signoff
    - Statistical, Simulation Based, and Scalable
- In-Situ Analog Reliability Verification
    - E.g., ensuring proper on-die LDO voltage regulation margin

Opportunities for Reliability Improvement

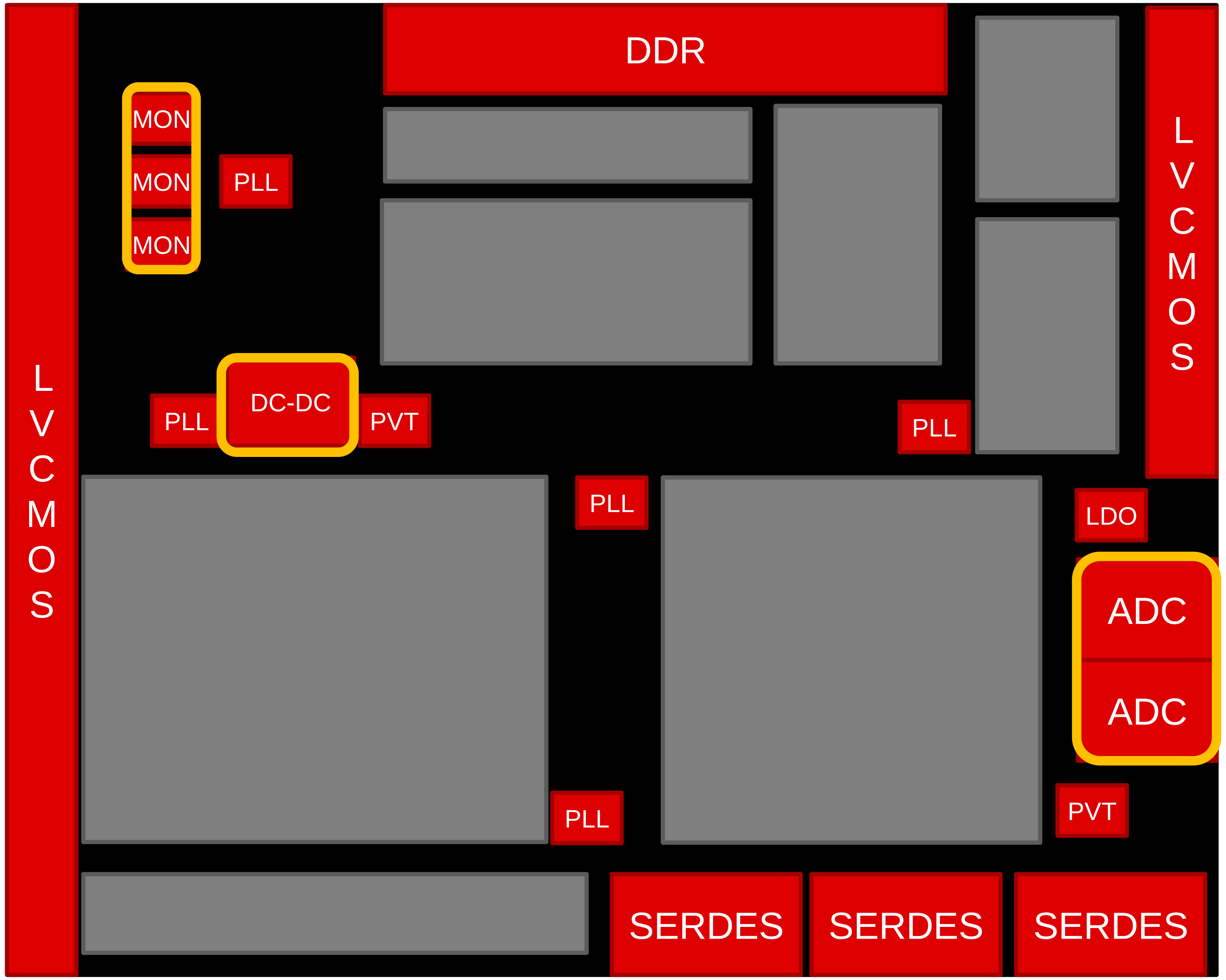


- Space large buffers to reduce local current, EM, and power grid FIT.
- Ensure large cells are near upper power-grid connections.
- Opportunistic improvements in power grid – power straps, redundant power vias.
- Proactive wire widening and redundant vias for improved signal EM.

Analog and Third-Party IP Integration

Analog Integration

- Significant analog content driven by end-market requirements
- Traditional Analog IP
  - SERDEs, DDR, LVCMOS (higher date rates)
- Monitoring
  - Process / Temperature sensors
- System Complexity
  - Integrated ADCs, power converters and regulators, etc.



Analog Integration Challenges

- Integration requirements often captured in PDF/DOC.
  - Custom routing sensitive analog signals including reference currents.
  - Substrate coupling ; keepout rules (analog vs. digital keep out)
  - Power supply routing / coupling.
  - PLL and clock jitter
  - ➔ Lack of standard formats to specify complex integration and timing requirements.
- Analog Models
  - Most of the time these are custom spice deck based models.
  - Design risks – especially for analog IP with significant digital content.
- Validation of analog parameters
  - Pseudo-synchronous / analog-like scenario handling in timing constraints
  - Verification of analog power-supply variation.
  - Spice-like analysis required for some connectivity.

Ecosystem IP Integration

- “Standard” Models (lib, LEF, etc.)
  - General QC gaps…. even within a single IP vendor.
  - No robust techniques for model checking.
  - Standard still open to interpretation

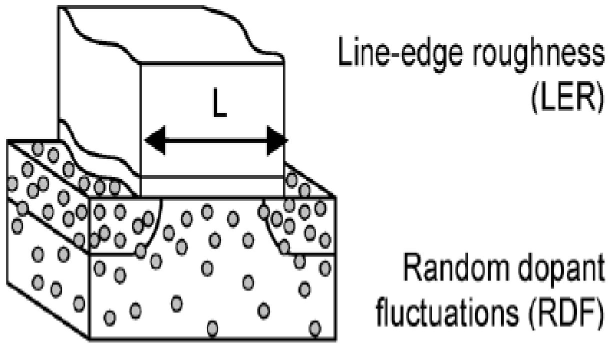
- Lack of Models
  - Similar to Analog, no formal methods to specify and check physical integration correctness.
  - E.g., no standard reliability models.

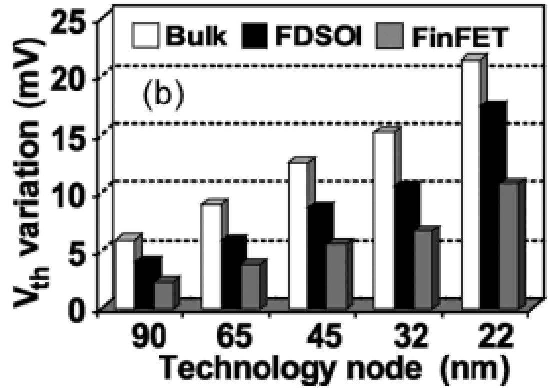
- IP Robustness
  - Spectrum of quality in the IP ecosystem.
  - Increasing risk to late stage ECO & bounding box changes.

Design Uncertainties and Outliers

Statistical Analysis and Optimization

- Random process variation is well known.
  - Gate work function, RDF, line-edge roughness, …
- Statistical timing has evolved and widely used.
  - Low Vdd in advanced nodes ➔ increased variation.
- **BUT… this is only one component of uncertainty and variation in design.**





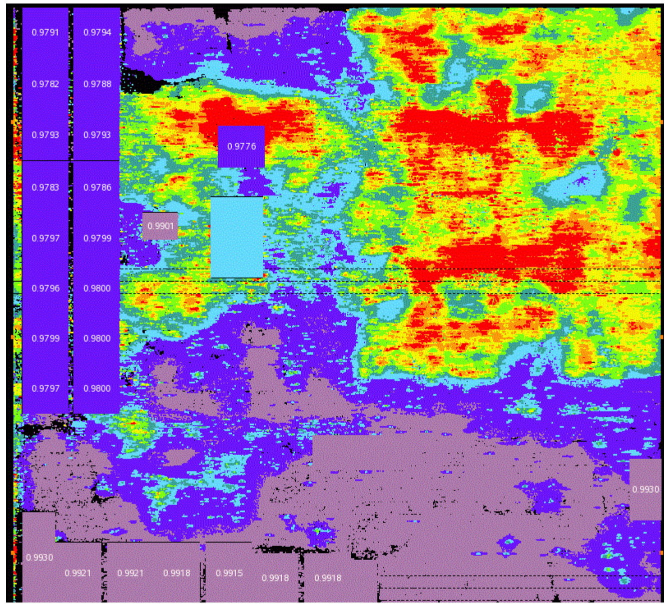
Hamed, Vivek, et al. IEEE transactions on Electronic Devices Vol.57, No.10, Oct-2010

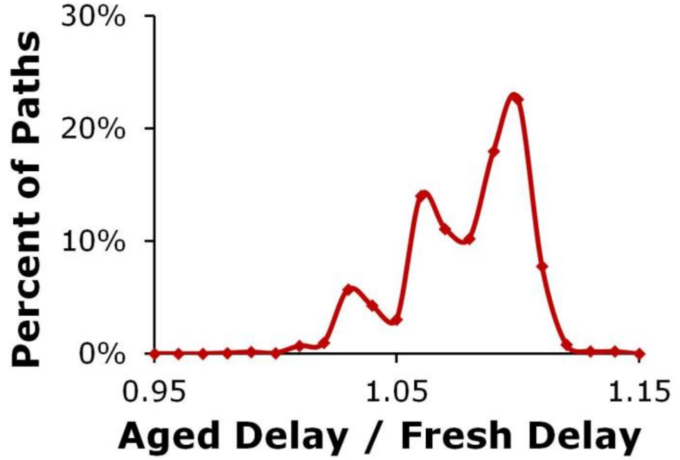
$$\Delta Td \sim \frac{1}{(Vdd - \Delta Vt)^n}$$

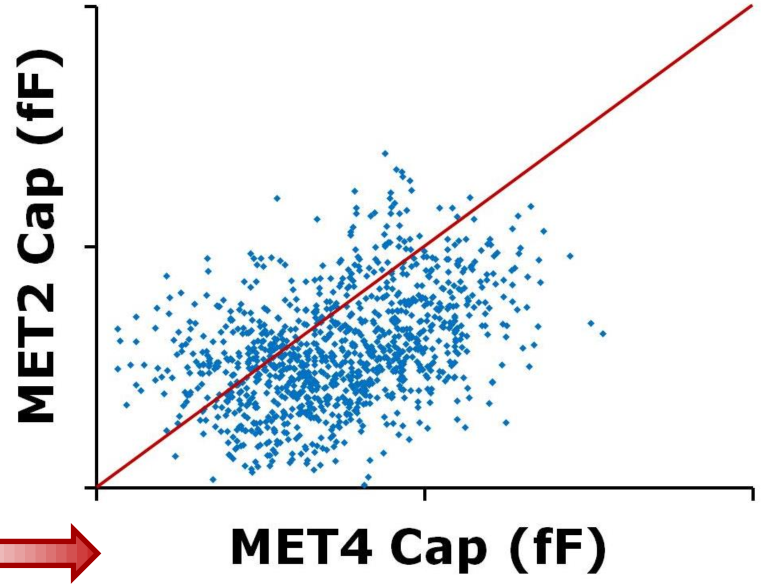
Uncertainties in Design

Effect
STA to Spice
Extraction Accuracy
Mismatch
Context
Dynamic and Static IR
SI – Coupling
Cross-Die Thermal
Cross Die Variation
Multiple Input Switching
Aging
Multi-Vt Skew
PMOS/NMOS Vt Skew
Metal Mismatch

Range	No. of Paths (Old)	No. of Paths (New)
-2% to -1%	0	2
-1% to 0%	0	39
0% to 1%	34	114
1% to 2%	175	370
2% to 3%	180	757
3% to 4%	471	471
4% to 5%	349	54
5% to 6%	528	5



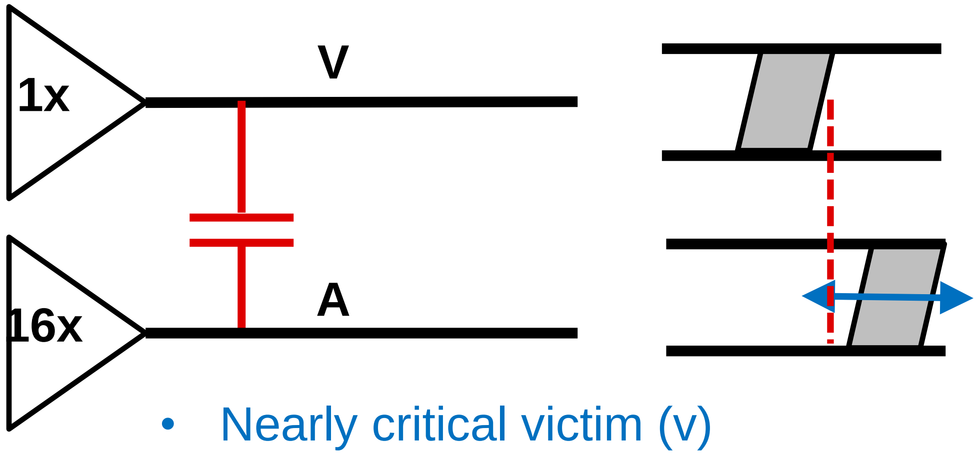




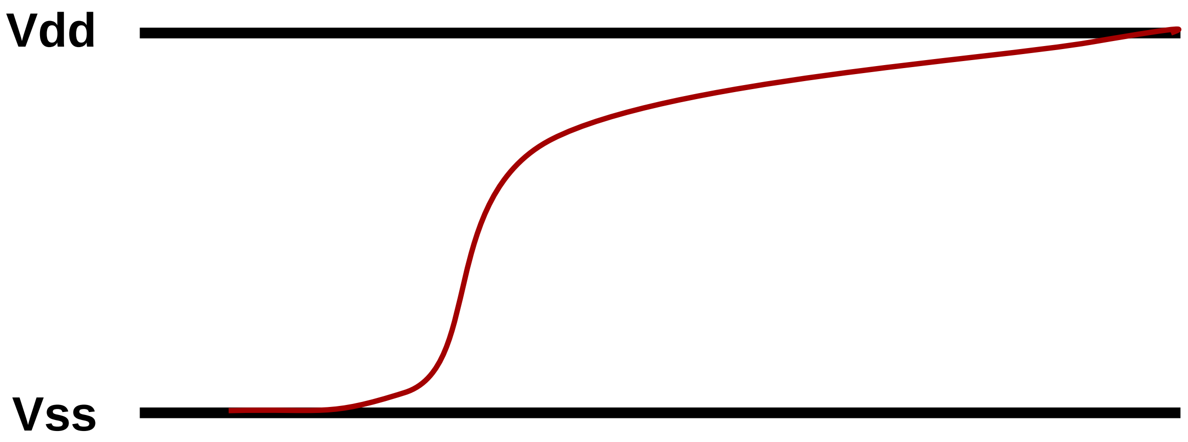
Motivation

- DPPM & FIT Attainment
  - Sensitive circuits are more prone to design uncertainties.
- Scenario Optimization
  - Advanced nodes and low voltage scenario explosion.
  - Eliminating sensitive circuits reduces scenarios which vary only in process, temperature, voltage, or interconnect corner.

Outlier & Sensitive Circuits



- Nearly critical victim (v)
- Aggressor (A) “just outside” window.
- Timing uncertainties
- ➔ possible overlap
- ➔ timing fail.



- Long tails often caused by under-driven nets
- May not switch rail-to-rail in a single clock cycle.
- Risk is inaccurate STA.

- Traditional STA (even statistical) misses many outlier circuit types.
- Solutions are ad hoc today based on user experiences (generally bad Si).
- Systematic approaches are needed (especially in the context of DPPM/DPPB designs)

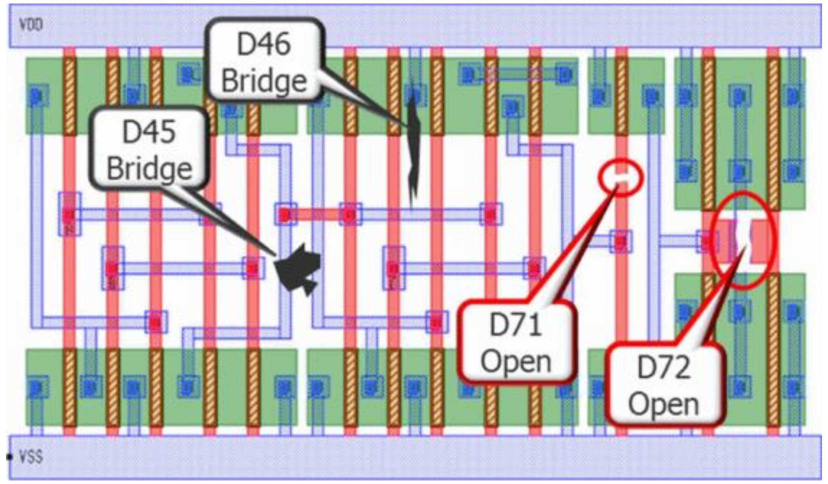
Opportunities in Uncertainty and Outlier Optimization

- Some ideas to eliminate sensitive circuits…
  - Limited wire length (and RC variation)
  - Strict max cap limits
  - Smarter use of small drive cells (tend to have most variation)
  - Limiting crosstalk (large bumps, noisy slews)
  - Crosstalk as a “design rule” in PD/signoff tools
  - Elimination uncertainty on clocks (SI, IR drop, etc.)
  - Controlling slew vs. slack (critical paths need tighter slew control)
  - Avoid “0 slack walls” – intelligently add positive timing margin

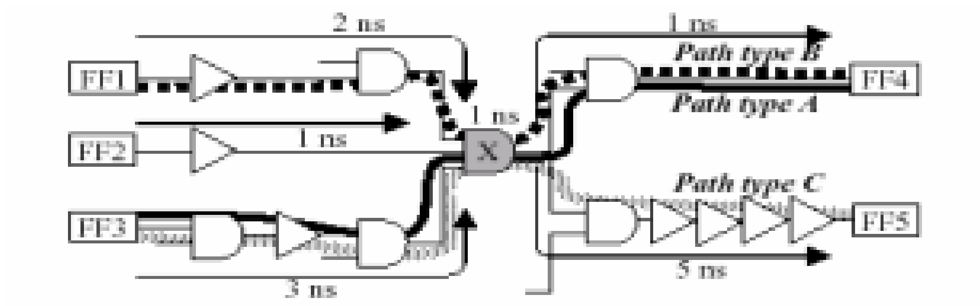
Design for Test

Design for Test

- Today: 0 DPPM ➔ Tomorrow: 0 DPPB (billion)!
- In-situ test required for safety and non-T0 failures.
- Higher coverage requirements as design complexity and quality requirements increase.
  - Cell Aware, Small Delay, ...
  - New fault models for 3D technologies.
  - More Analog integration, analog fault models, and new safety analysis.



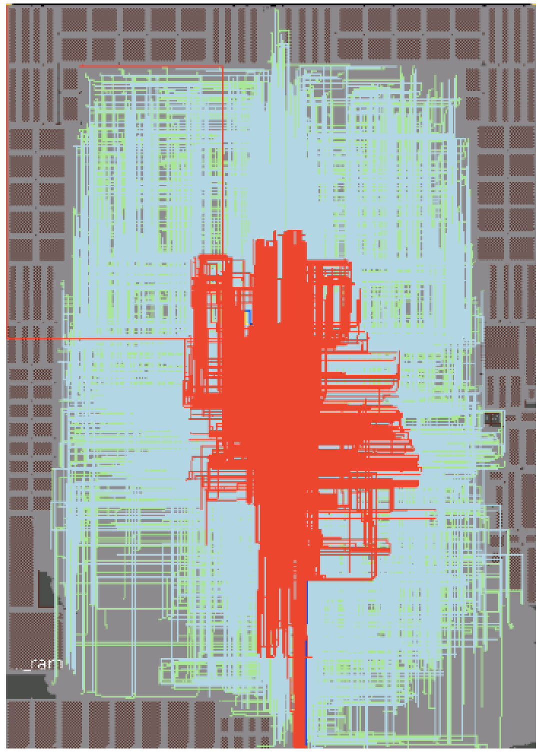
Cell Aware ATPG & Diagnosis, Maxwell & Hapke '16

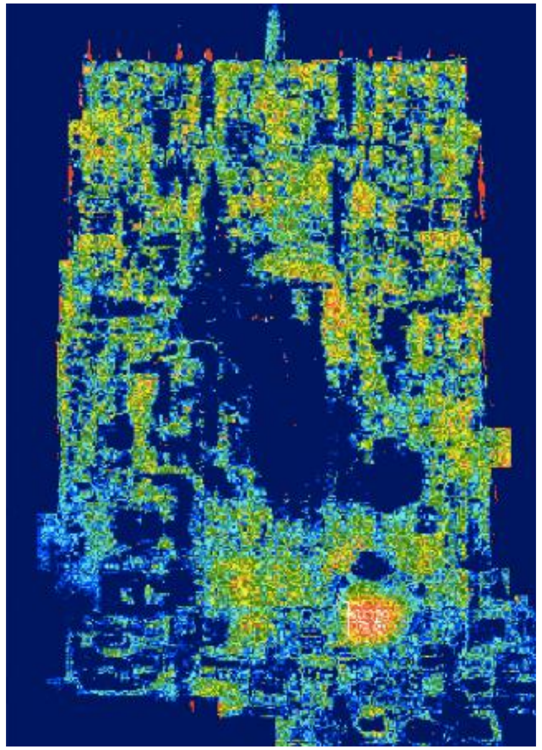


Small Delay Defects, Uzzaman'09

Design for Test – Physical Design Impact

- DFT **WAS**
  - Scan chains (long, low frequency)
  - Simple memory test
- DFT **IS**
  - 1000s of short scan chains
  - Multiple compressors
  - Logic BIST, Transition Fault Coverage
- Impact to Physical Design
  - Compressor optimization, scan reordering, BIST routing and optimization.
  - Test power and power grid optimization.
  - Late insertion of observation points (registers)
  - Logic optimization for improved observability (e.g., XOR trees)
  - Matching functional and test path delays.





Design-for-Test PD Opportunities

- Fault-aware place and route
  - Minimize *unobservable* faults.
  - Late insertion of observation points (registers)
  - Logic optimization for improved observability (e.g., XOR trees)

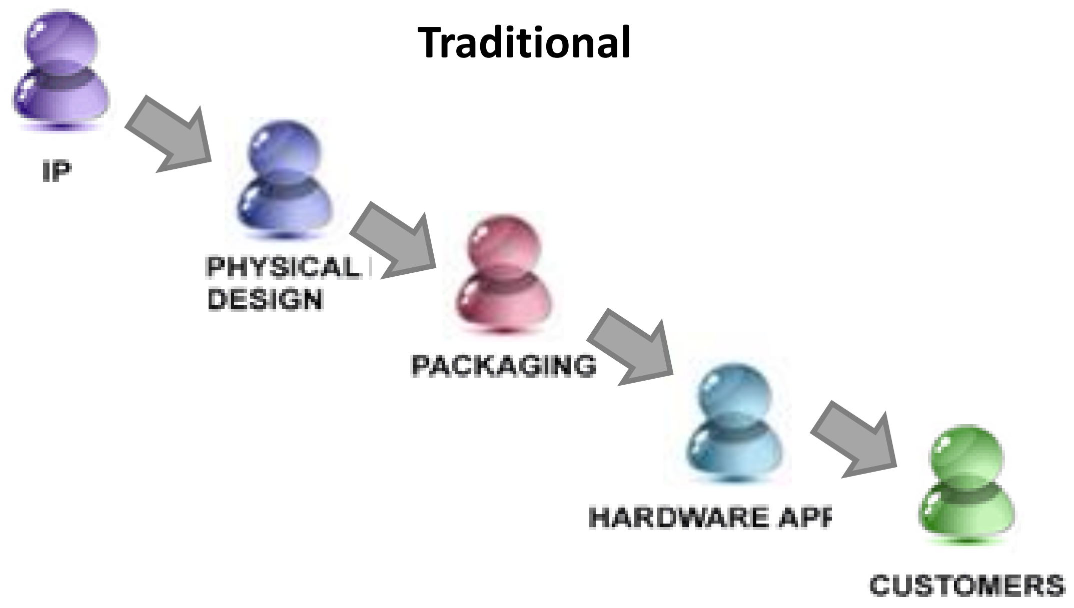
- Low-Power ATPG
  - High coverage ➔ High activity ➔ Over-Designed Power Grid
  - How do we spread logic to reduce peak power during ATPG?

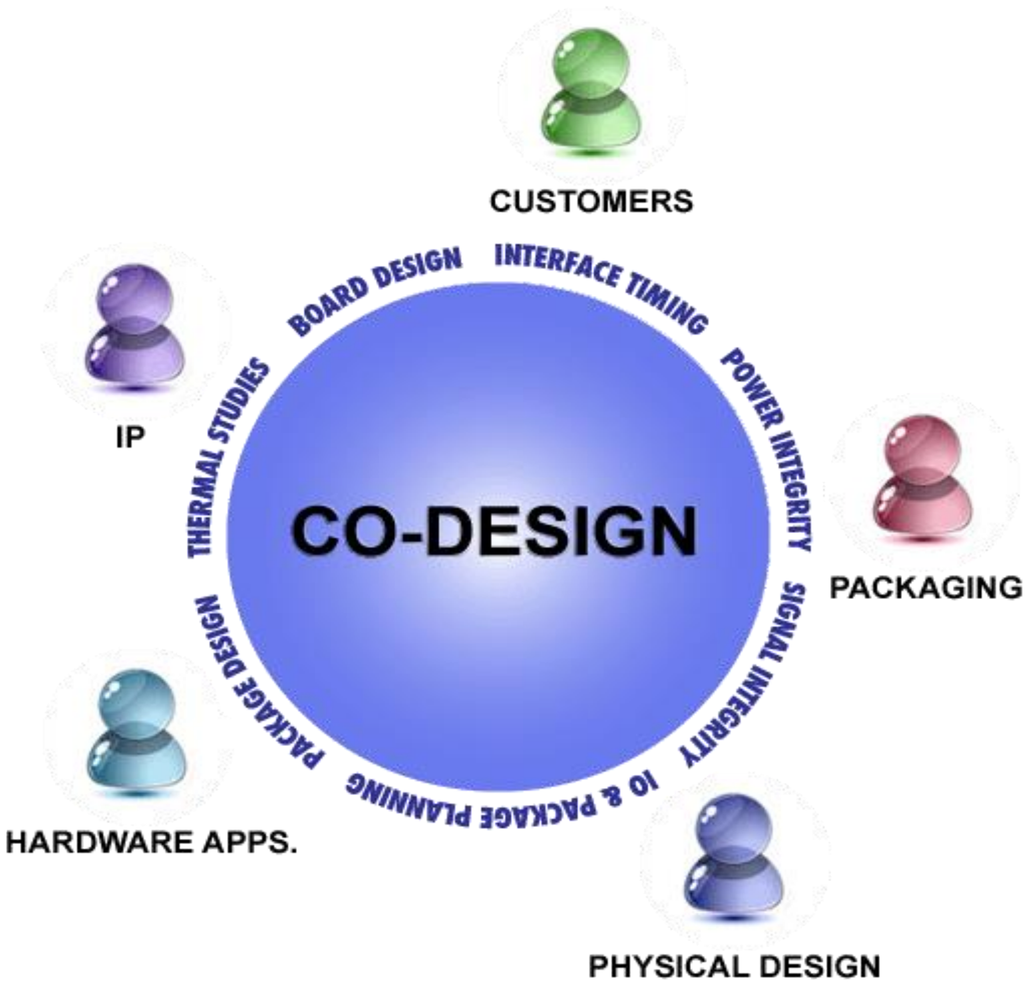
- Tool needs for better QOR/Schedule
  - Elegant handling of large number of scan chains.
  - Physical-aware logic compressor handling.

Package Co-Design

SOC-Package Co-Design Evolution

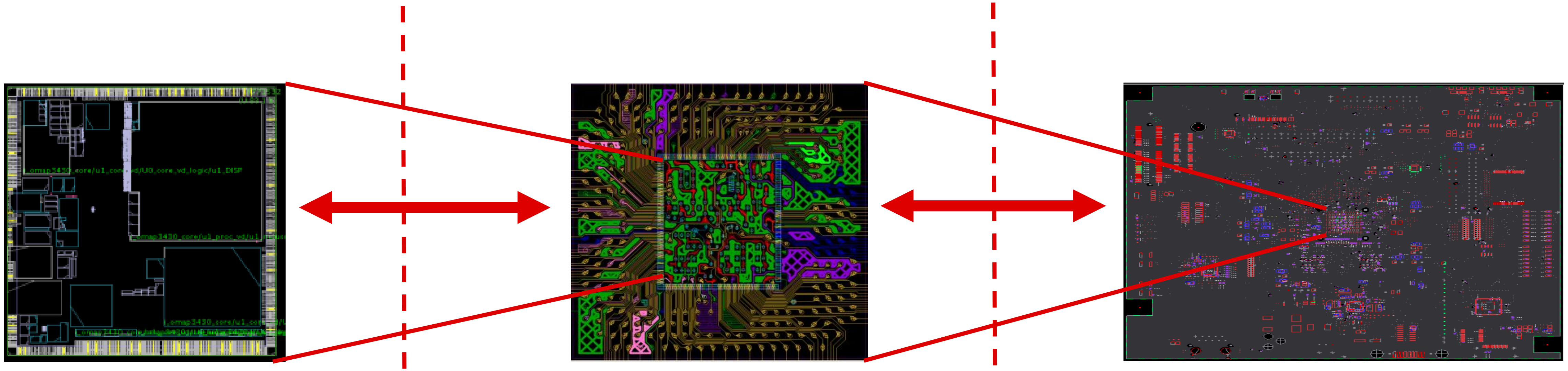
Traditional





Getting performance entitlement requires board and package down to IP and physical design view.

System Co-Design



- **Cost**
  - Die Size
- **Power**
  - Voltage Domains
- **Performance**

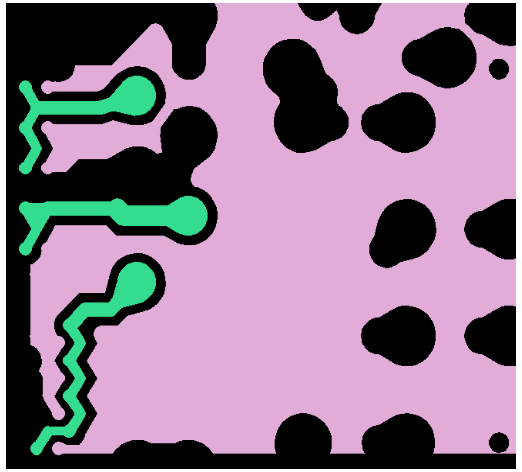
- **Cost**
  - Type, Size, Stackup
- **Power**
  - Lid vs no Lid
- **Power Integrity**
- **Pkg Reliability**
- **Pkg Thermal**
  - Hot Spots/Tj

- **Board Cost**
  - Stackup
  - Component Count
- **Signal Integrity**
- **Power Integrity**
- **System Thermal**

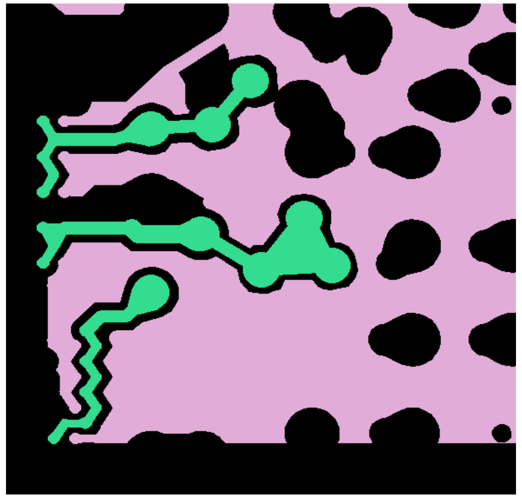
Die-Pkg **Pkg-Board**

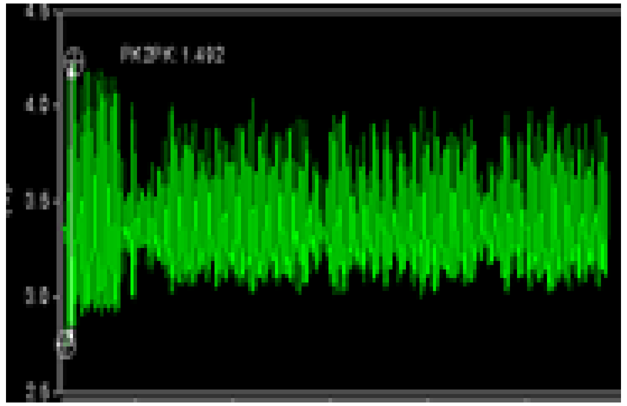
Package/Physical Co-Design for Reliability

Original



Modified





Result

Interface	P2P Noise
Original	2.02V
Modified	1.49V

The Average fail rate (AFR):

$$AFR\ FIT = -\frac{\ln(1-F(t))}{T} \propto V^n$$

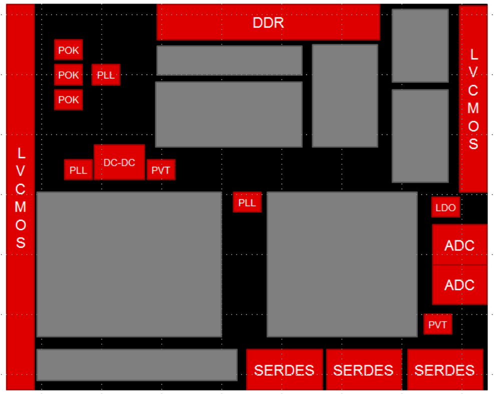
FIT Rate improved 64X!

- Co-optimizing floorplan, bumps, voltage domains with package routing is critical for reliability.

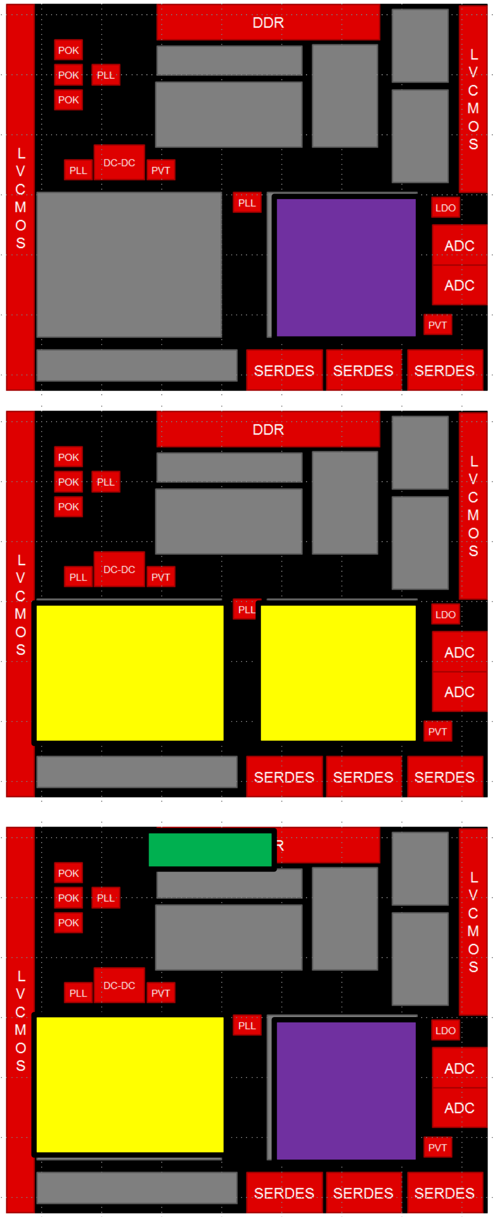
Design for Reuse

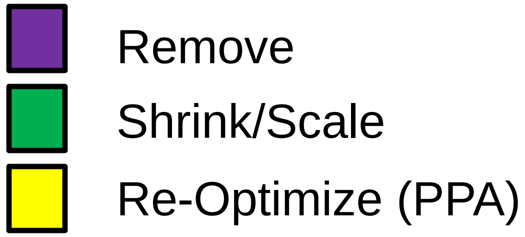
Design Reuse: Myths and Realities

"Master" SOC



Derivatives

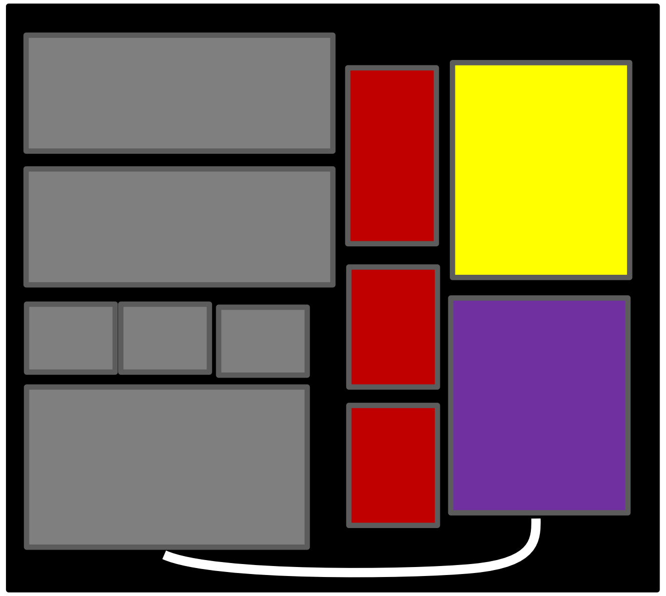




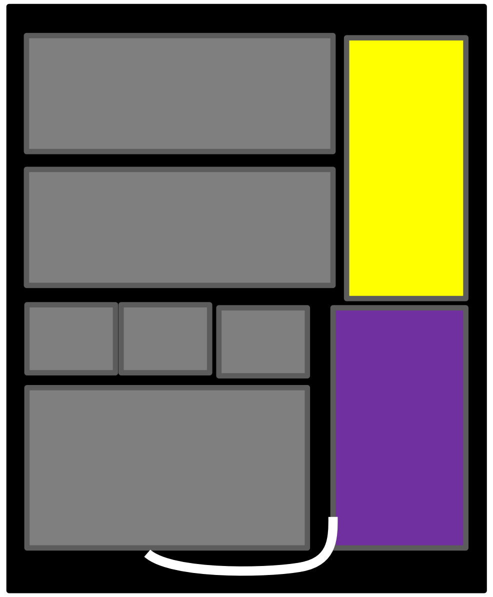
- Scope
  - Remove blocks (e.g., GPU)
  - Shrink/Scale for bandwidth (e.g., DDR)
  - Re-target lower PPA (e.g., CPU)
- Myths
  - "Remove x mm2 ➔reduce die by x mm2"
  - Re-Tape in weeks
- Realities
  - Reshaping blocks ➔ large floorplan changes.
  - Re-placing IO ➔ IO timing and package change
  - Top-level timing re-closure.
  - Block interface timing re-closure

Design for Re-Use Opportunities

- "Fuzzy Re-Optimization"
  - Idea: Automated morphing of previously optimized blocks
  - Reuse placement (as much as possible)
  - Pin/port movement and IO cone re-optimization
  - Automated macro movement and power grid



- Block Optimization to Maximize Re-Use
  - Even blocks which don't need re-shaped often can't be reused.
  - Constraint generation for re-use.
    - Ensure best possible timing on interface timing paths.
    - Maximize margin for simultaneous min-max timing



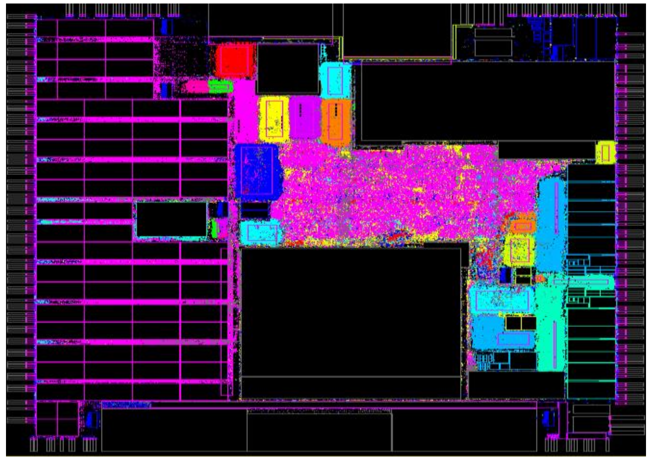
Grab Bag Opportunities

Application-Specific Optimizations

Example: SOC Buffering

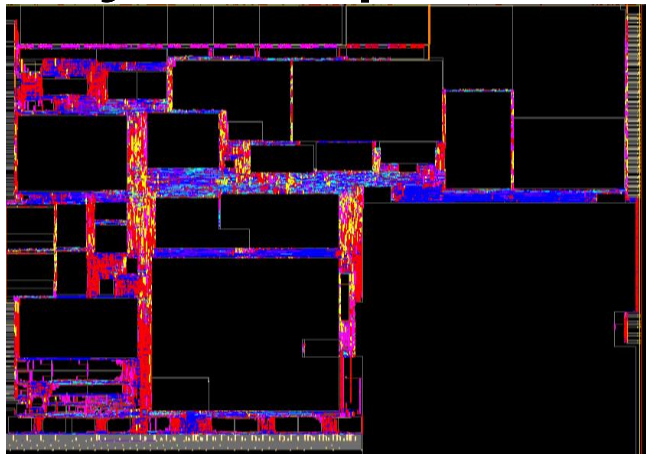
Control

Classic P&R



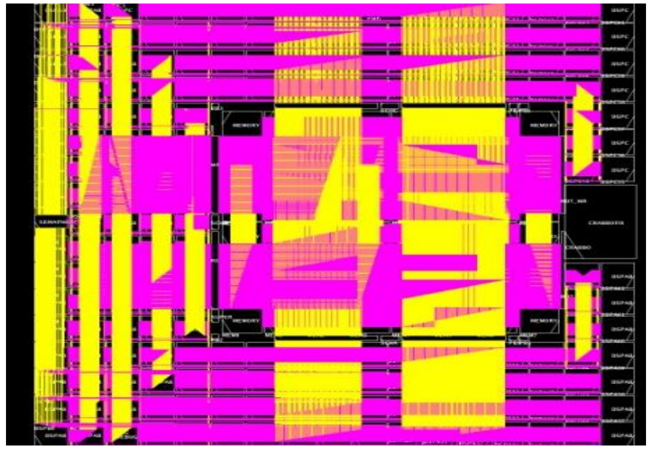
- Synthesized repeaters
- Auto routed wires

Cycle Optimal



- “Application-specific optimization”
- Planned repeaters
- Auto-routed wires
- Ultra-fast cycle time (~couple hours)

Fully Planned

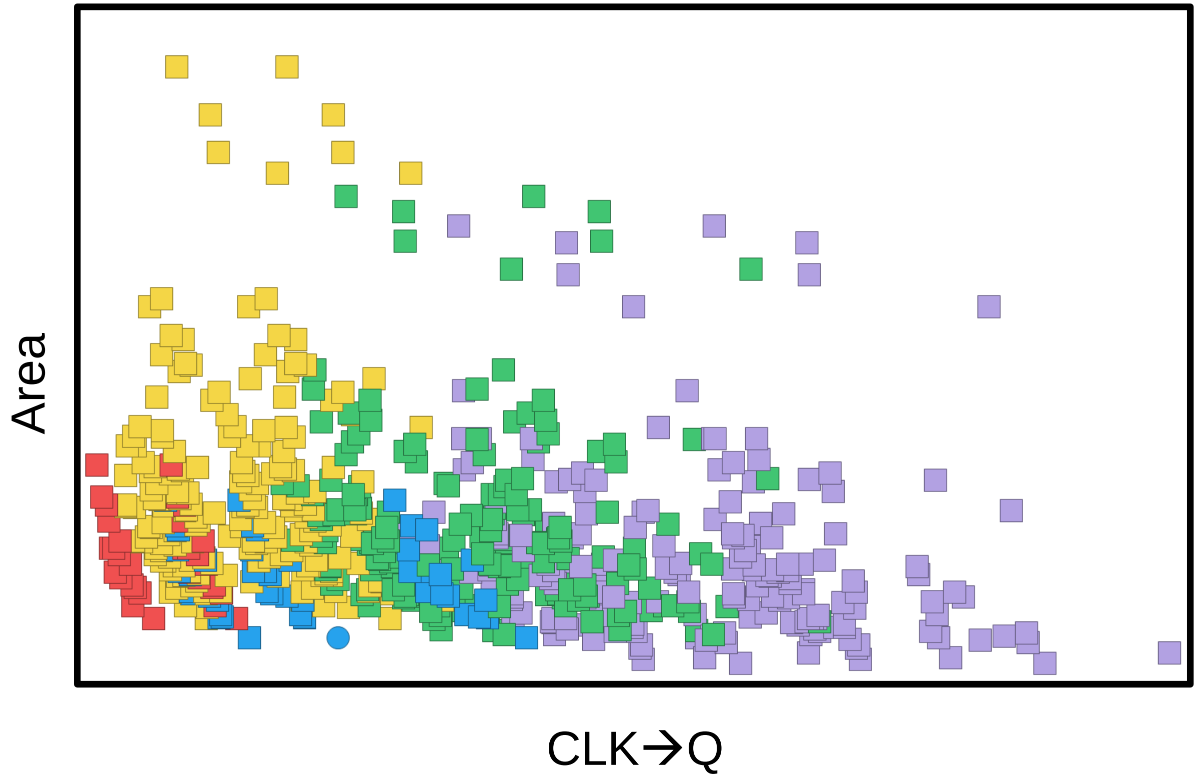


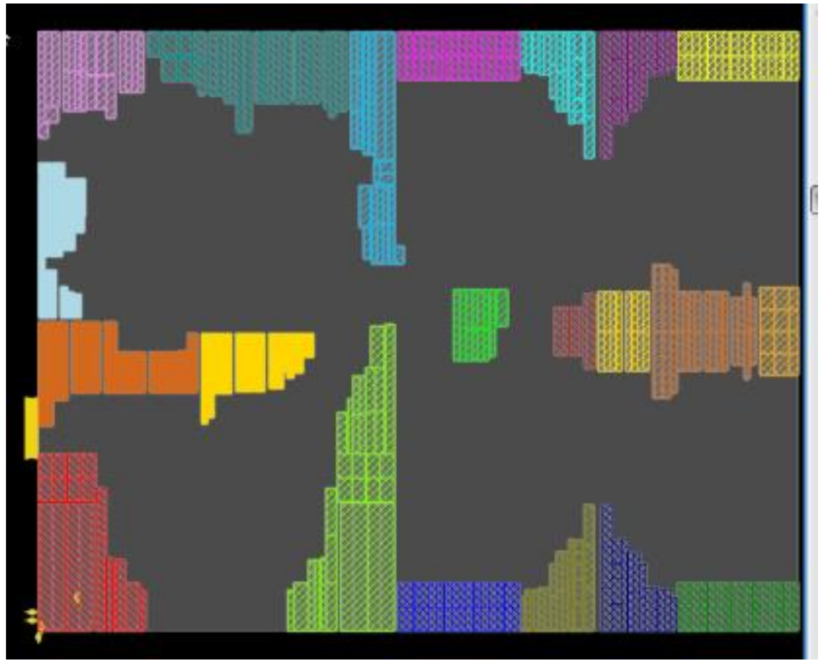
- Planned repeaters
- Planned wires
- Excellent PPA; long TAT.

Effort

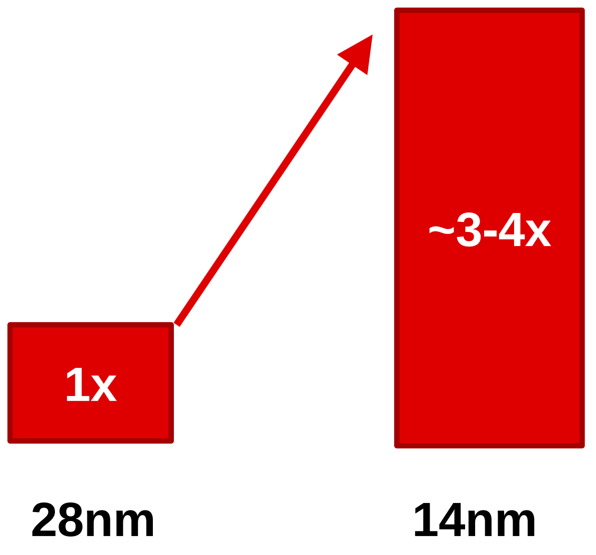
SRAM Optimization

- SRAM selection now similar to standard cell optimization.
  - HP vs. HD bit cells
  - uLVT, LVT, SVT decode
  - MUX factor
  - Center Decode
- Optimal selection is an evolving PD problem.
  - Significant PPA impact with proper selection.
  - Difficult problem
    - Complex floorplans around macros.
    - Requires some automation in power routing
- Automatic SRAM/macro placement.
  - Blocks with 1000s of macros ➔ automation!

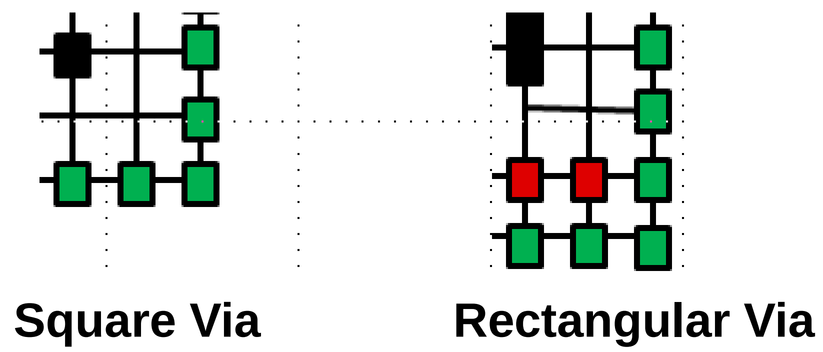




Complex DRC Handling and Fixing

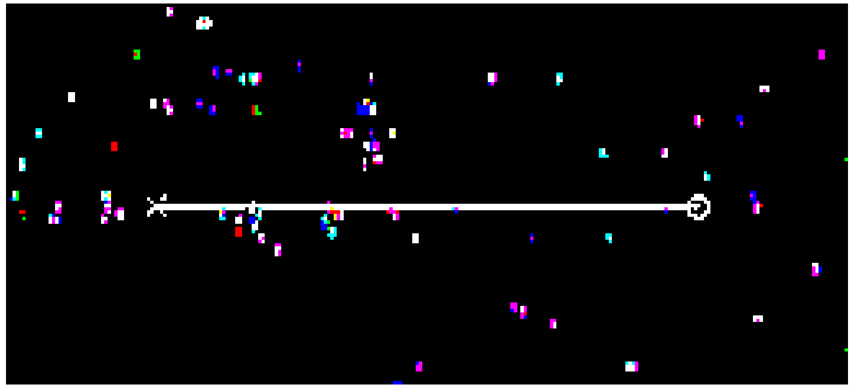


New DRC Types
- Double-pattern masks
- Mid-end-of-line metal
- More min-area rules
- …



- Design rule complexity exploding at advanced nodes.
- P&R tools can't comprehend all complex rules within inner optimization loops.
- Designers struggle to fix complex rules by hand.
- Need better "signoff-quality" rule fixing and native understanding in algorithms.

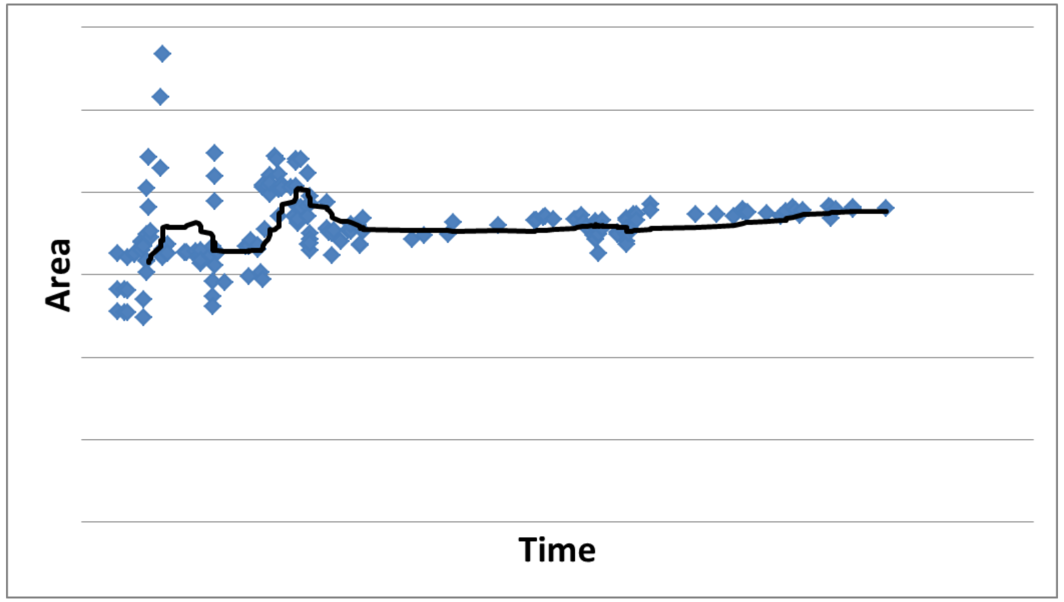
Congestion & Post-Route Closure



- Complex DRCs make pre-route congestion estimation more challenging.
  - Multiple adjacent gcells “on the edge” of routability.
  - Complexity in estimating resources.
  - Complex power grid/signal interaction.

- More reliance on advanced post-route techniques or margin.
  - ➔ Need more tricks or better predictability.
  - E.g., carry knowledge of ‘potential slack’ on nets to routing.

Dirty Data



- Numerous iterations on sub-chips/IP during SOC development.
- EDA TAT typical focus is in a clean "regression" setup
- Often design planning uses very early data - design netlists, constraints etc.
- Opportunity here to improve PD experience/QOR with early design data and re-use data from early runs to improve convergence and learning cycles.
  - E.g., last run this endpoint needed margin due to congestion; feedback to placement.

Summary

Summary of Physical Design Challenges

- IP Integration: Analog and Ecosystem
- Reliability: Calculators and Algorithms to Improve Reliability
- Uncertainty-Based Signoff
- DFT: Reduced PPA Impact and PD-Driven DPPM Reduction
- Package Co-Design: Bringing Board and Package Earlier into SOC Design
- Design for Re-Use
- Application-Specific Optimization Techniques
- SRAM Optimization: Selection and Macro Placement
- DRC Closure and Route Predictability in Advanced Nodes
- Dirty Date / Iterative Design