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Analog Placement Constraint Extraction and Exploration with the Application to Layout Retargeting

Biying Xu[1], Bulent Basaran[2], Ming Su[2], David Z. Pan[1]

[1] ECE Department, University of Texas at Austin

[2] Synopsys, Inc

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Outline

- Introduction
- Proposed Layout Retargeting Framework
  - ✓ Analog Placement Constraint Extraction
  - ✓ Constraint-aware Placement
- Experimental Results

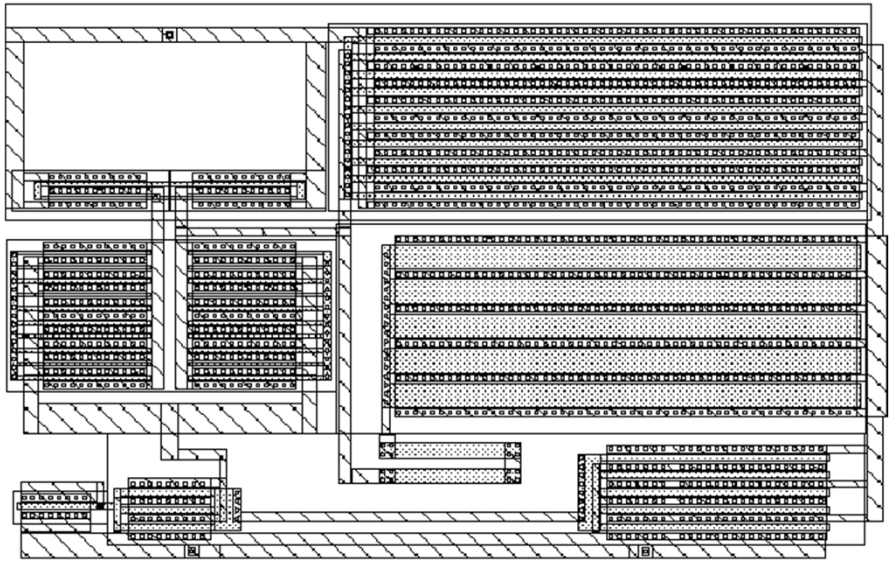
Analog/Mixed-Signal Integrated Circuit

- Rapid growth of the analog/mixed-signal integrated circuit (AMS IC) market
  - ✓ consumer electronics, automotive, Internet of Things (IoT)…
- Increasing layout design complexity in the advanced technology nodes
- Present AMS IC layout design is heavily manual
  - ✓ time-consuming and error-prone
  - ✓ calls for design automation for AMS ICs

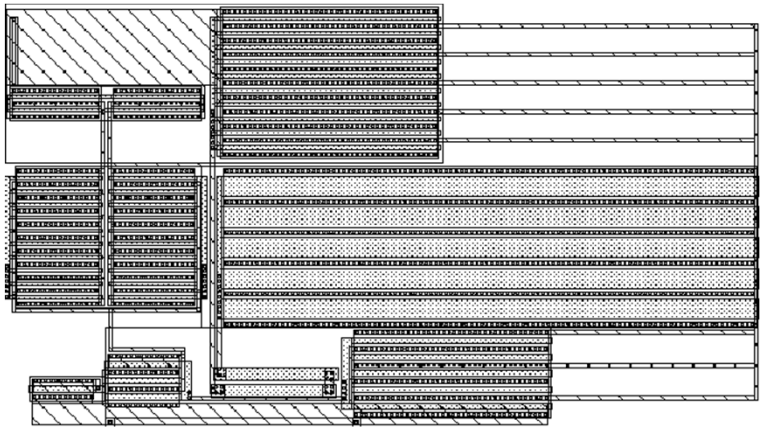
"Although the analog circuit area is usually less than 20%, its required design efforts can be more than 80%." -R. Rutenbar

Analog Layout Retargeting

- Reuse previous high-quality, well-optimized layouts
  - ✓ apply design knowledge in existing layouts
  - ✓ reduce manual design efforts
- Technology migration & performance retargeting



Original layout in 0.25-um technology

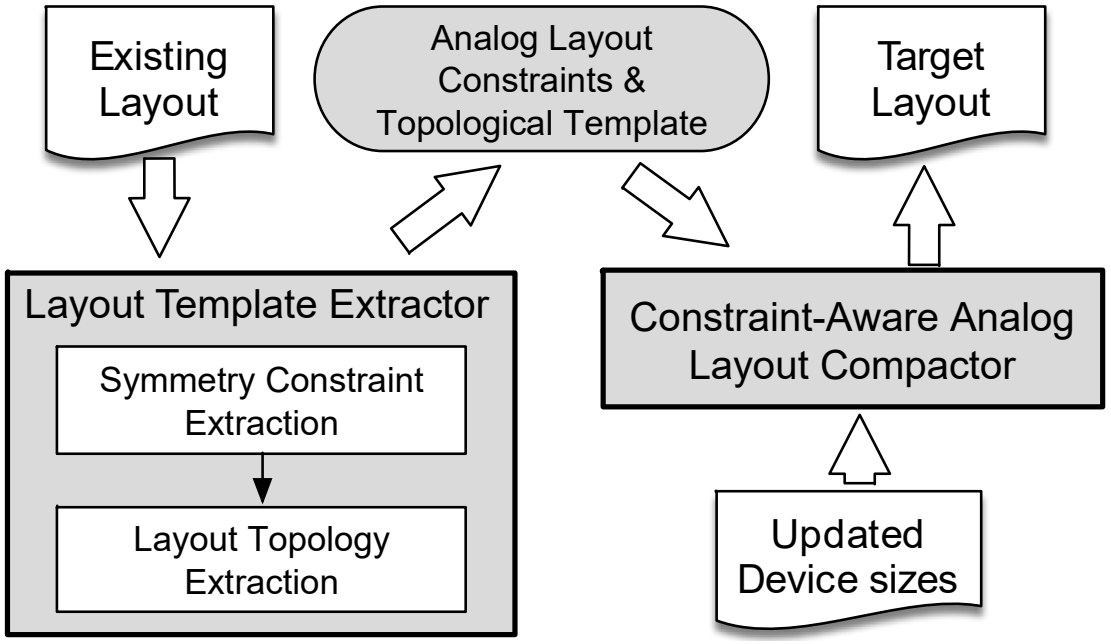


Targeted layout in 0.18-um technology

Courtesy of [X. Dong+, TCAD'16]

Prior Work

- MASH [F.-L. Heng+, ISPD'97]
- IPRAIL [N. Jangkrajarng+, 2003]
- Others [Z. Liu+, ASPDAC'10], [P.-C. Pan+, TCAD'15], [X. Dong+, TCAD'16], [X. Dong+, ISCAS'17]
- Same layout topology; some layout constraints not captured



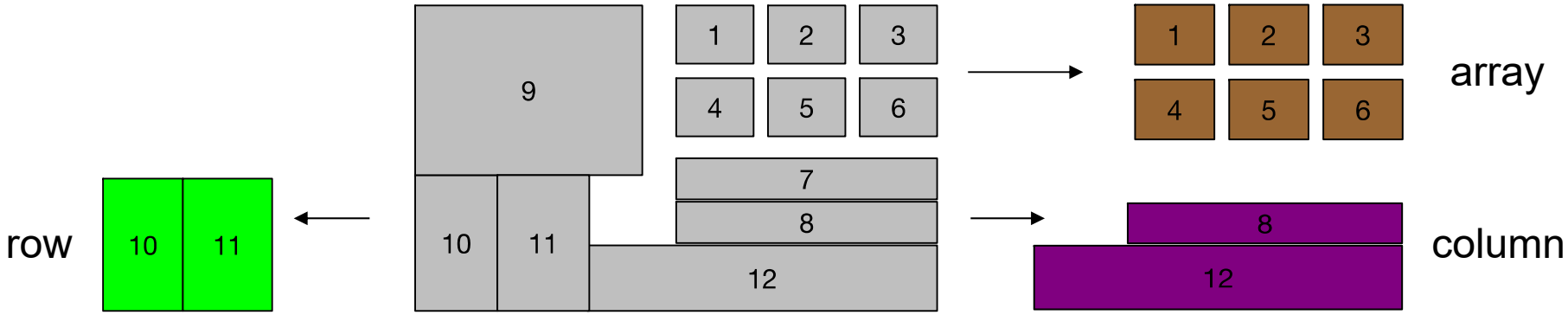
Conventional Layout Retargeting Flow

Our Contributions

- A novel layout retargeting framework is proposed to preserve the symmetry and regularity constraints in the existing layout
- For the first time, an efficient sweep line-based algorithm is developed to extract all the regularity constraints in an analog placement
- Experimental results show that the proposed layout retargeting framework can reduce the placement area compared with the conventional approach

Analog Layout Constraint

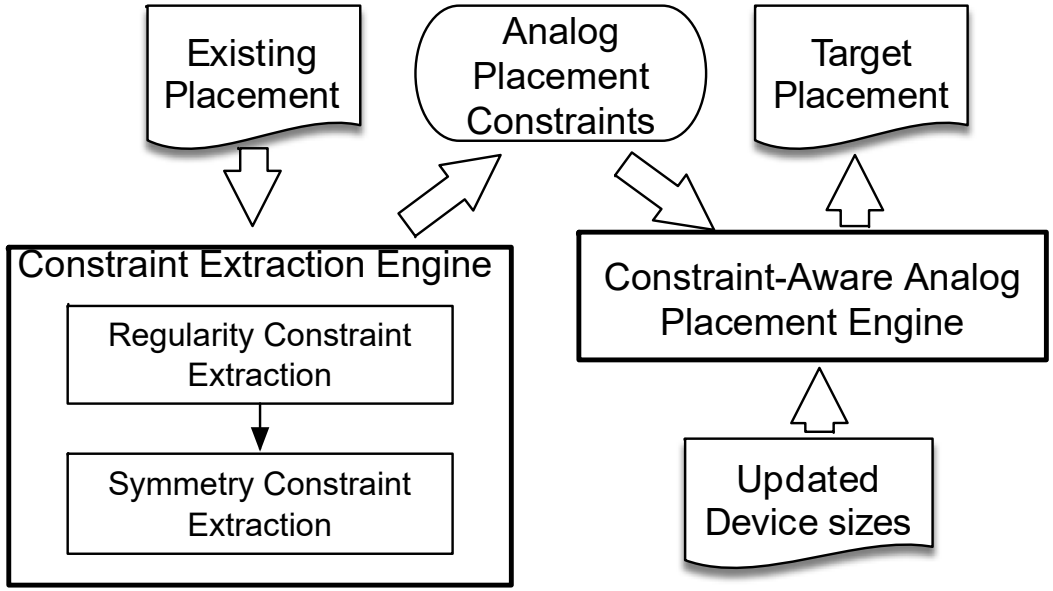
- Regularity constraints
  - ✓ Topological rows, columns, and arrays
  - ✓ Improve routability, minimize #vias on the critical wires, and reduce circuit performance degradation [S. Nakatake, ASPDAC'07], [S. Nakatake+, ASPDAC'10]



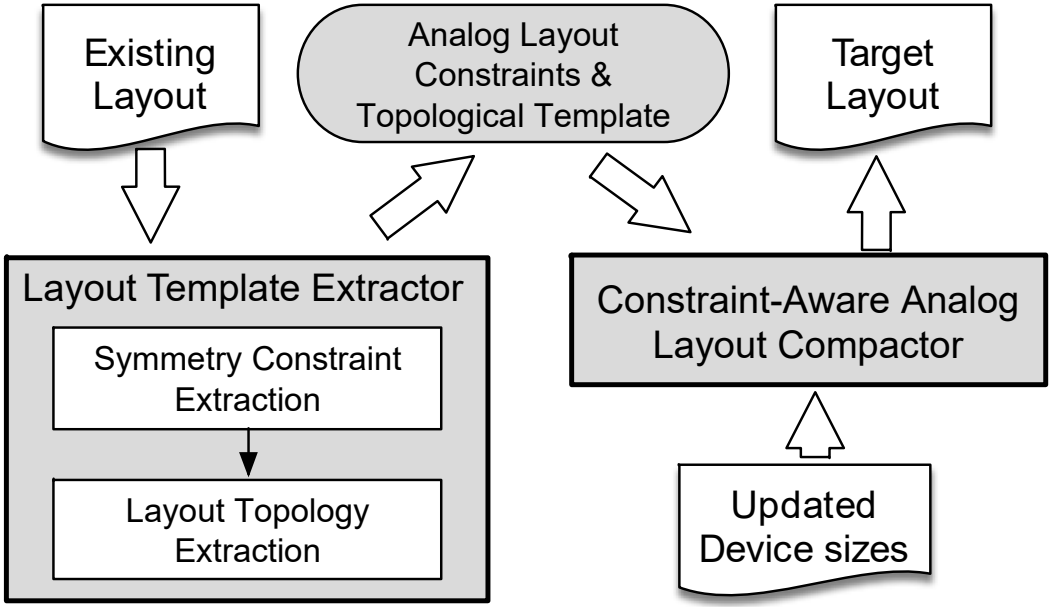
- Symmetry constraints
  - ✓ Algorithm in [N. Jangkrajarng+, 2003]

Proposed Layout Retargeting Flow

Proposed Approach

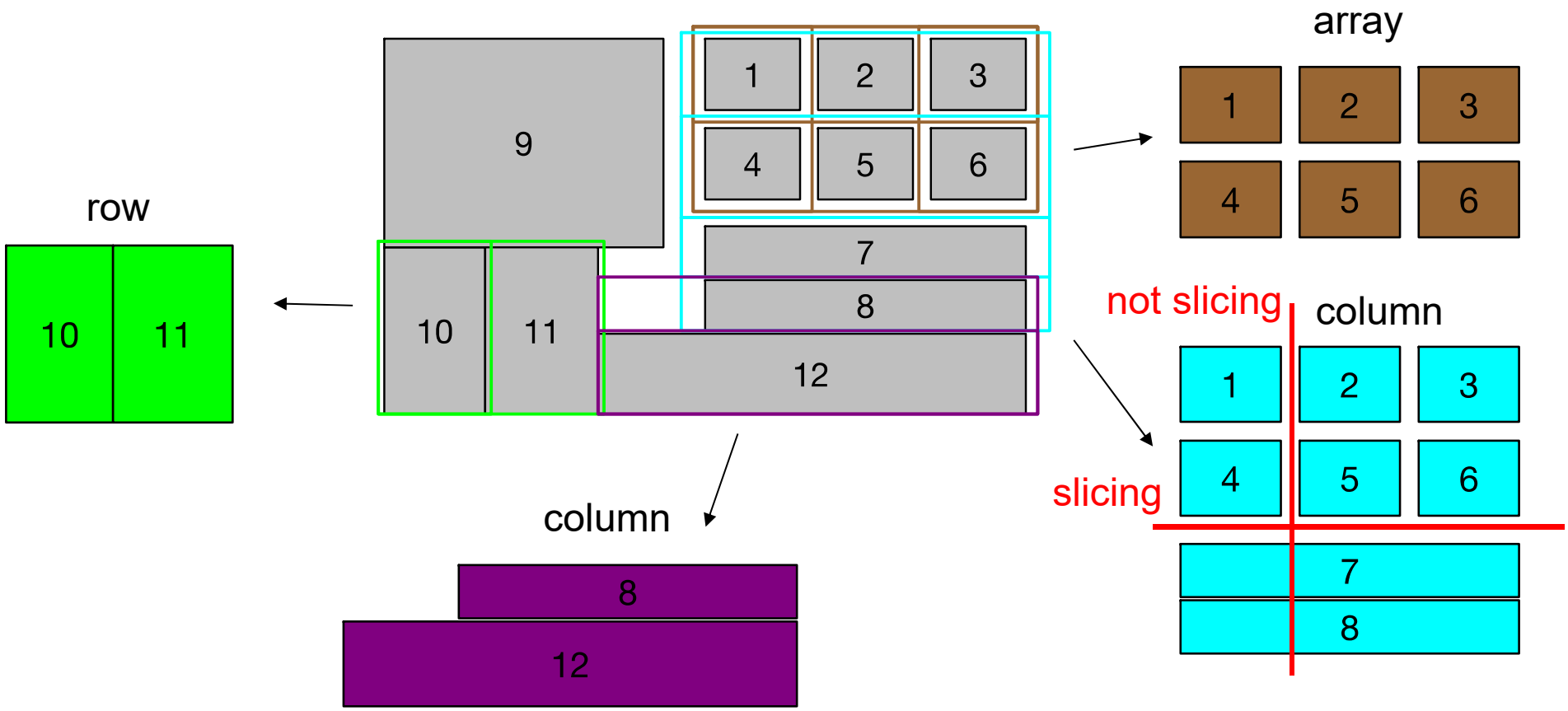


Conventional Approach



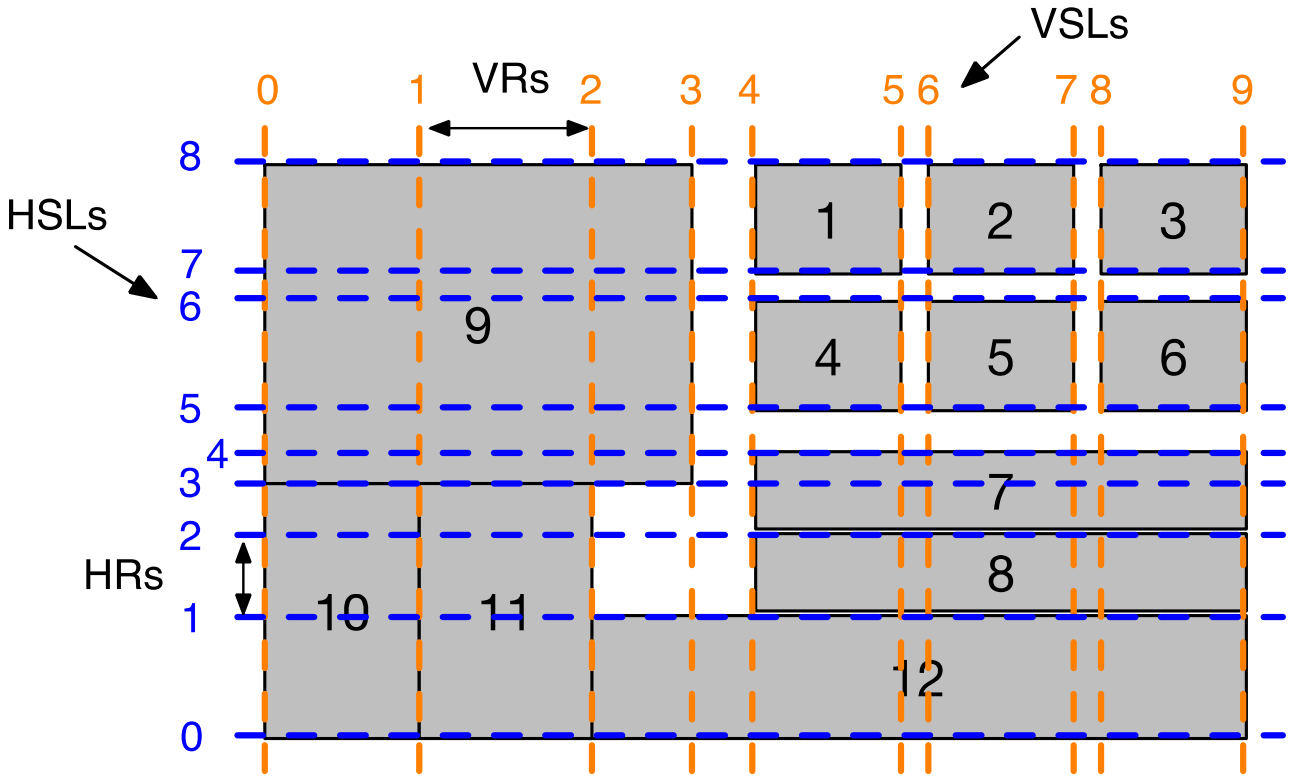
Regularity Constraint Extraction

- Goal: extract all the non-dominated regular structures
- Dominance: the set of slicing lines of one regular structure ⊆ that of another regular structure



Sweep Line-Based Approach

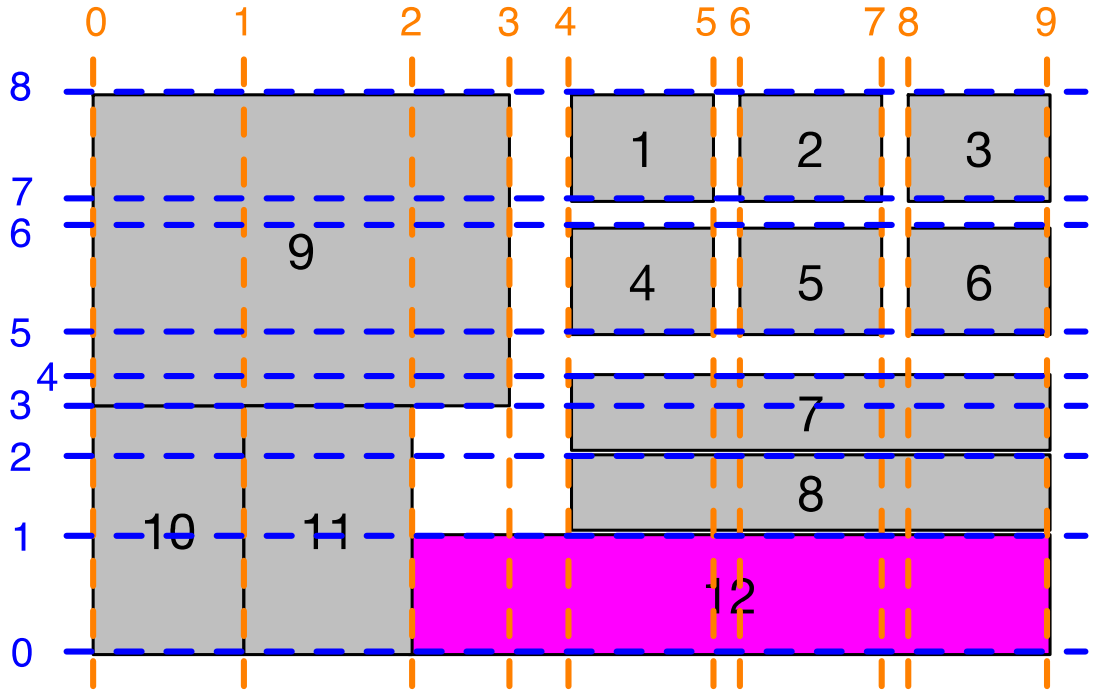
- Horizontal / Vertical slicing line: HSL / VSL
- Horizontal / Vertical region: HR / VR



Hanan Grid

Boolean Lookup Tables (LUTs) (1)

- V_{dr} and H_{dr}: regions a device occupies



VRs → V_{dr}

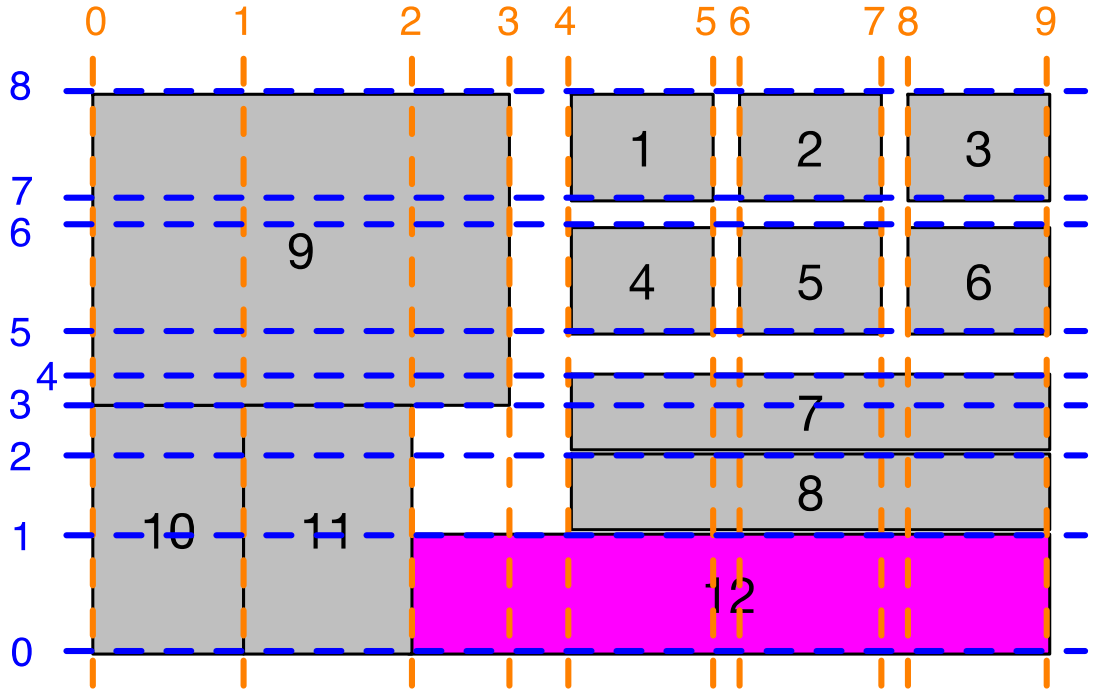
devices	0	1	2	3	4	5	6	7	8
1	0	0	0	0	1	0	0	0	0
2	0	0	0	0	0	0	1	0	0
...					...				
12	0	0	1	1	1	1	1	1	1

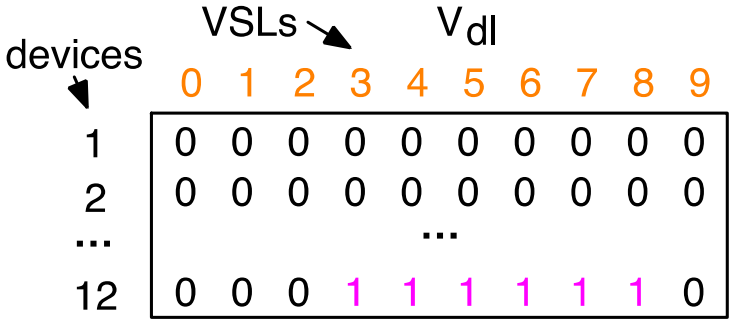
HRs → H_{dr}

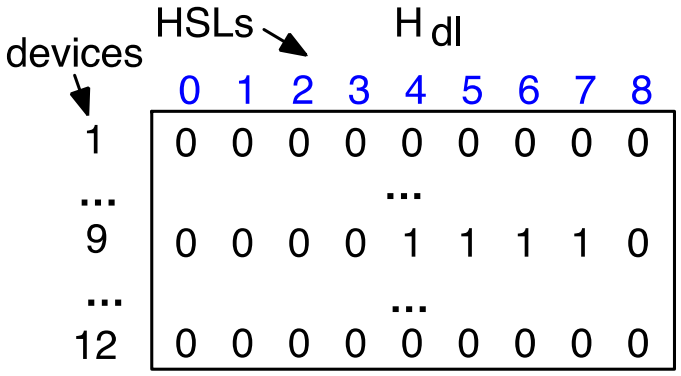
devices	0	1	2	3	4	5	6	7
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	1
...					...			
12	1	0	0	0	0	0	0	0

Boolean LUTs (2)

- V_{dr} and H_{dr}: regions a device occupies
- V_{dl} and H_{dl}: slicing lines a device strictly intersects

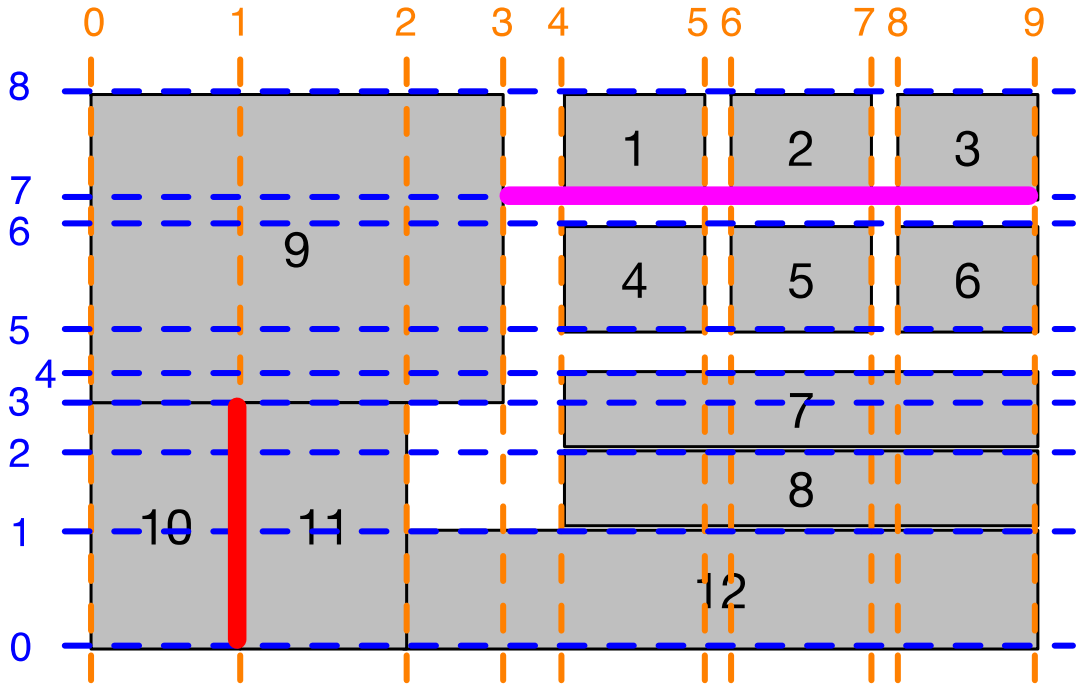


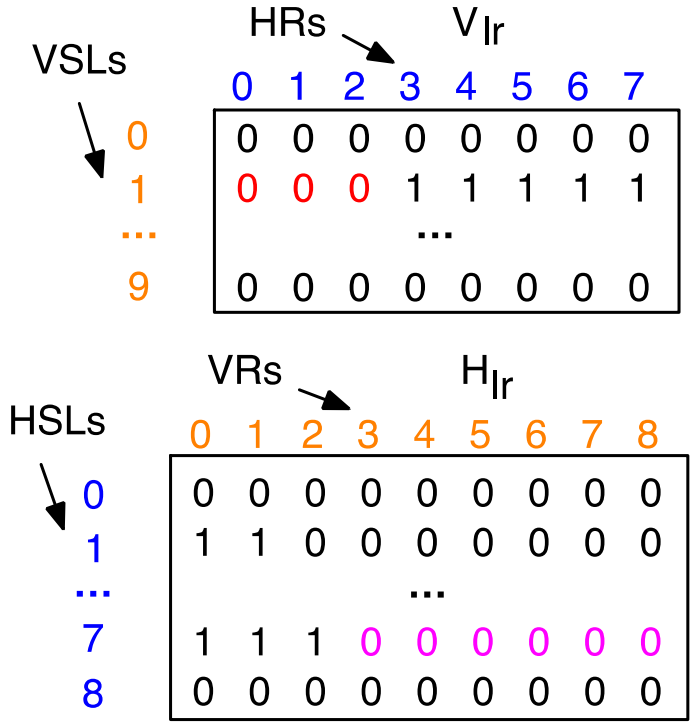




Boolean LUTs (3)

- V_{dr} and H_{dr}: regions a device occupies
- V_{dl} and H_{dl}: slicing lines a device strictly intersects
- V_{lr} and H_{lr}: regions where a slicing line strictly intersect any device

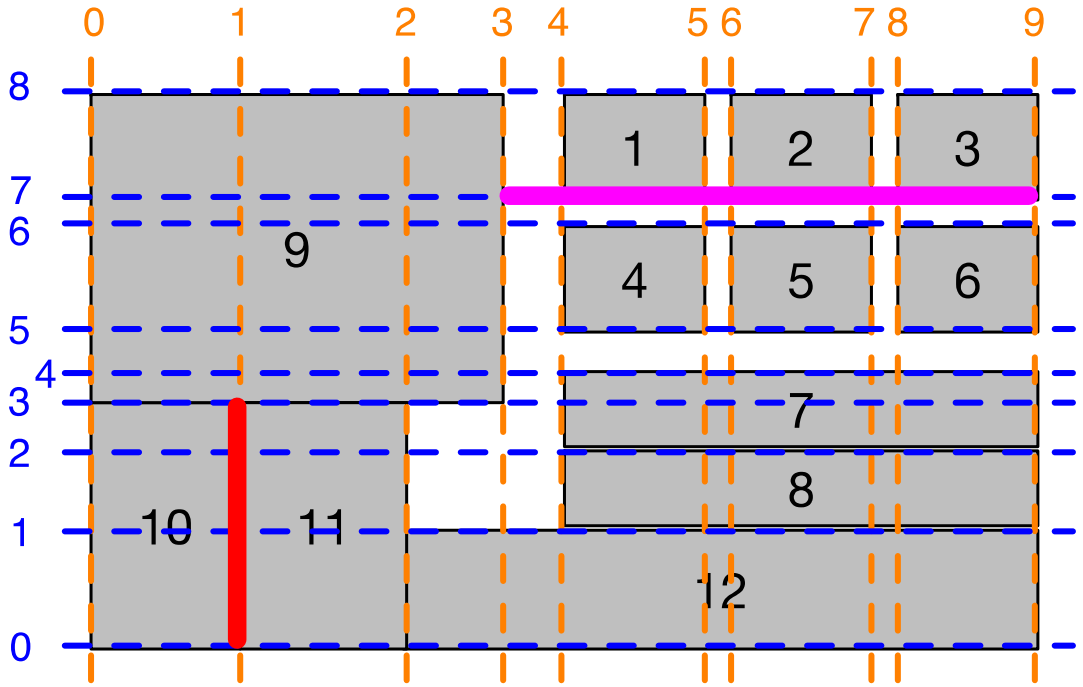


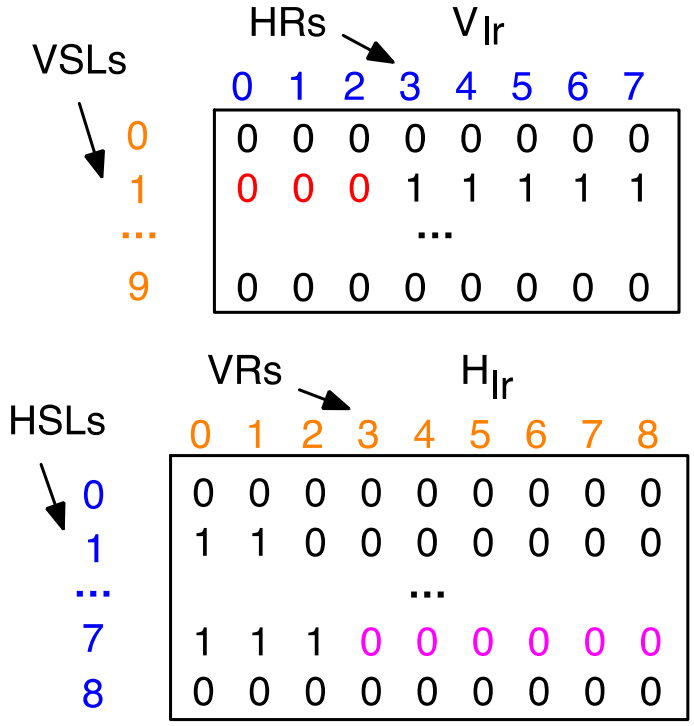


Boolean LUTs (3)

Observations

- ✓ The j^{th} HR is slicing at the i^{th} VSL iff $V_{lr}[i][j]$ is 0.
- ✓ The j^{th} VR is slicing at the i^{th} HSL iff $H_{lr}[i][j]$ is 0.

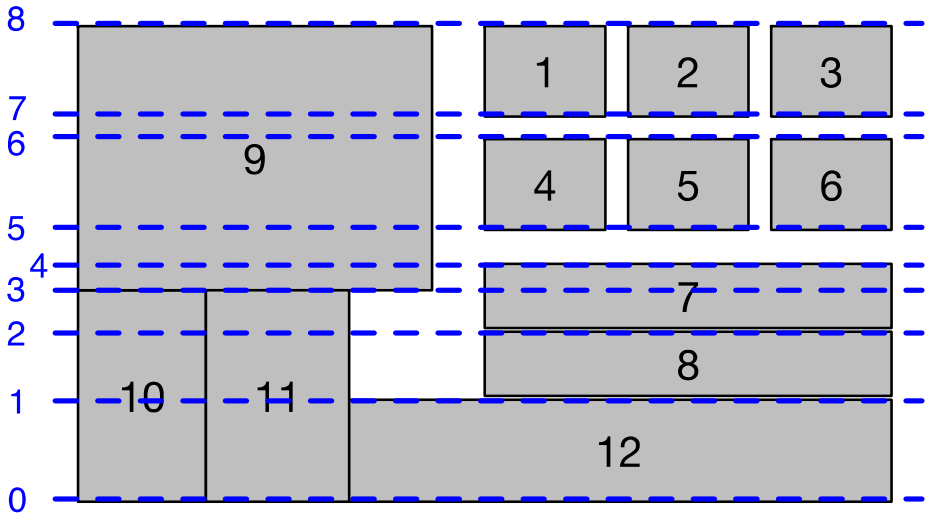




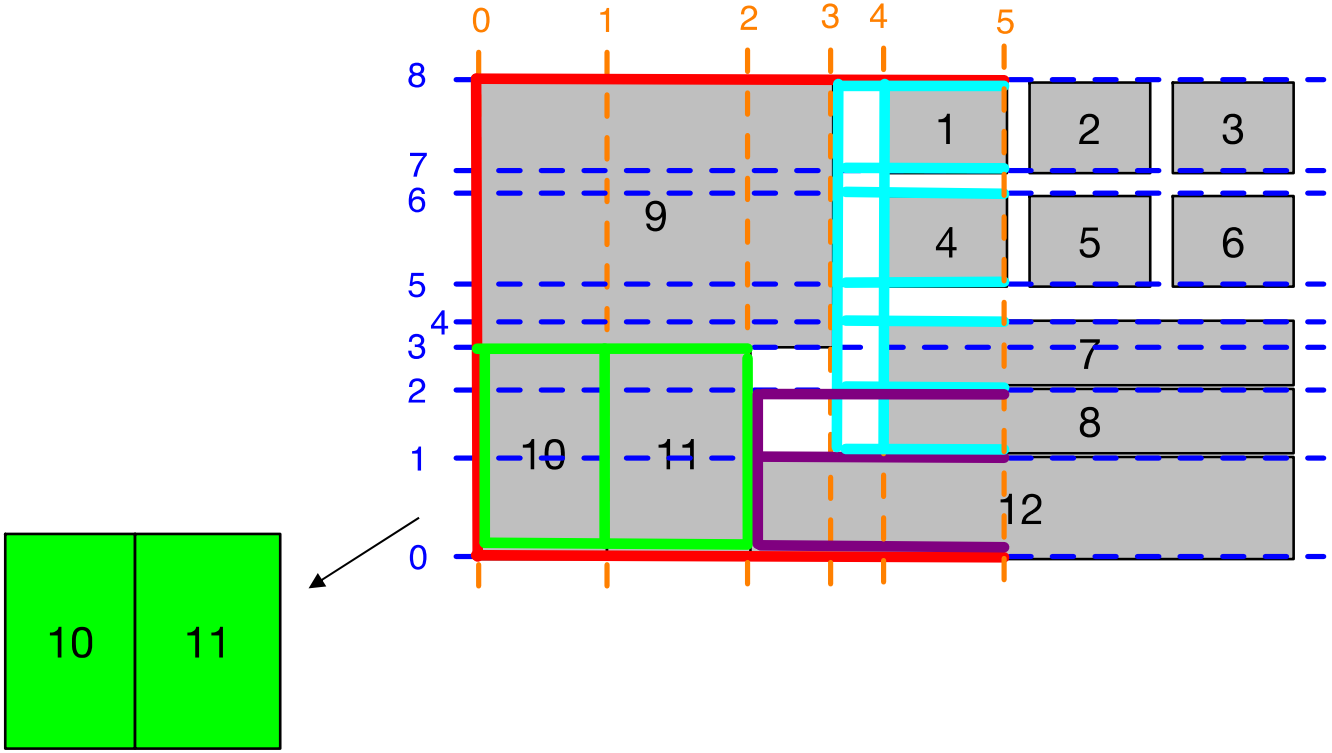
Sweep Line-Based Algorithm

- Sweep all the vertical slicing lines from left to right
- Get the slicing segments from the LUTs V_{lr} and H_{lr}
- For each intermediate regular structure
  - ✓ add_vertical_slicing_line
  - ✓ delete_horizontal_slicing_lines
  - ✓ add_non_dominated_regular_structure
- For each vertical slicing segment
  - ✓ add_intermediate_regular_structure

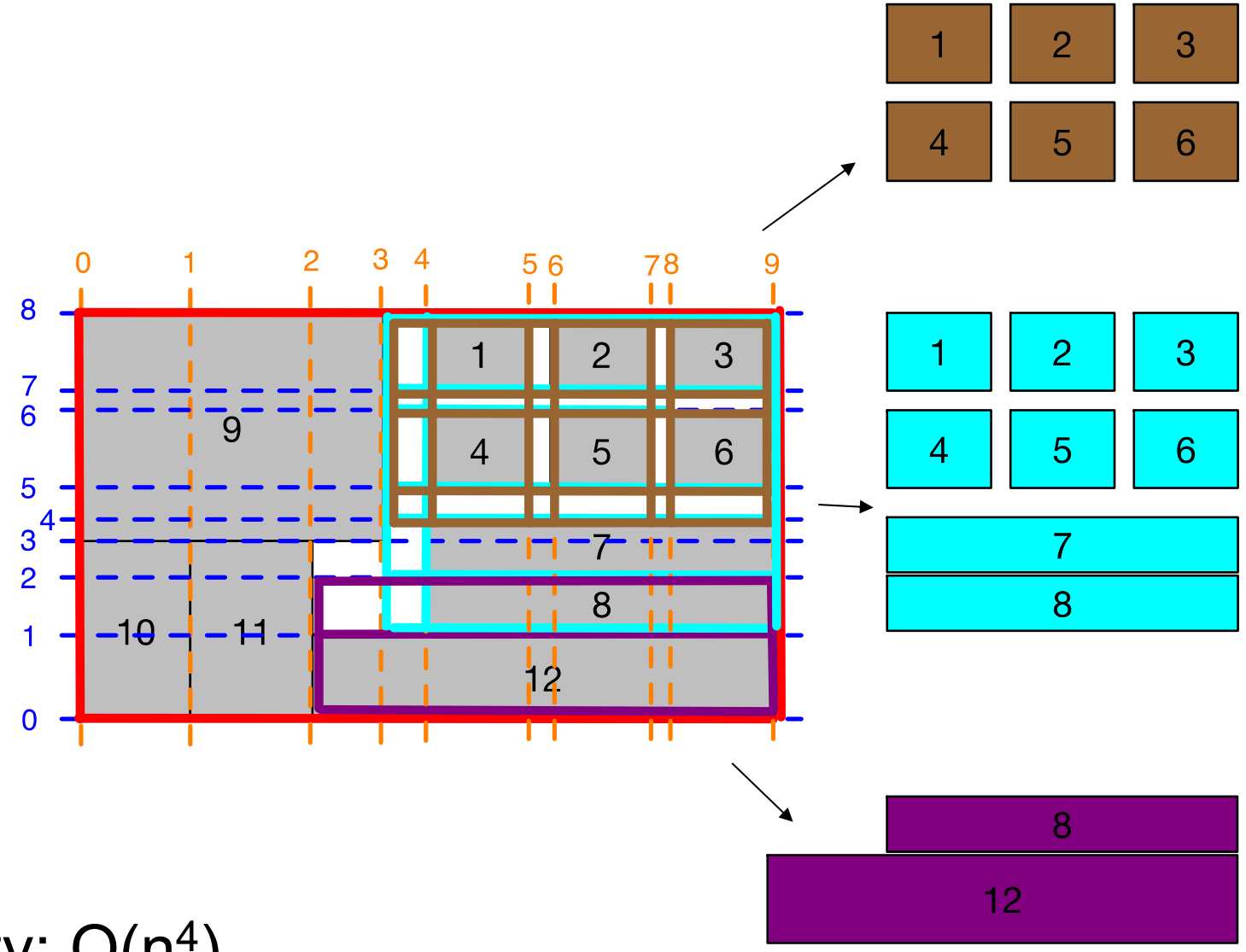
Sweep Line-Based Algorithm Example



Sweep Line-Based Algorithm Example

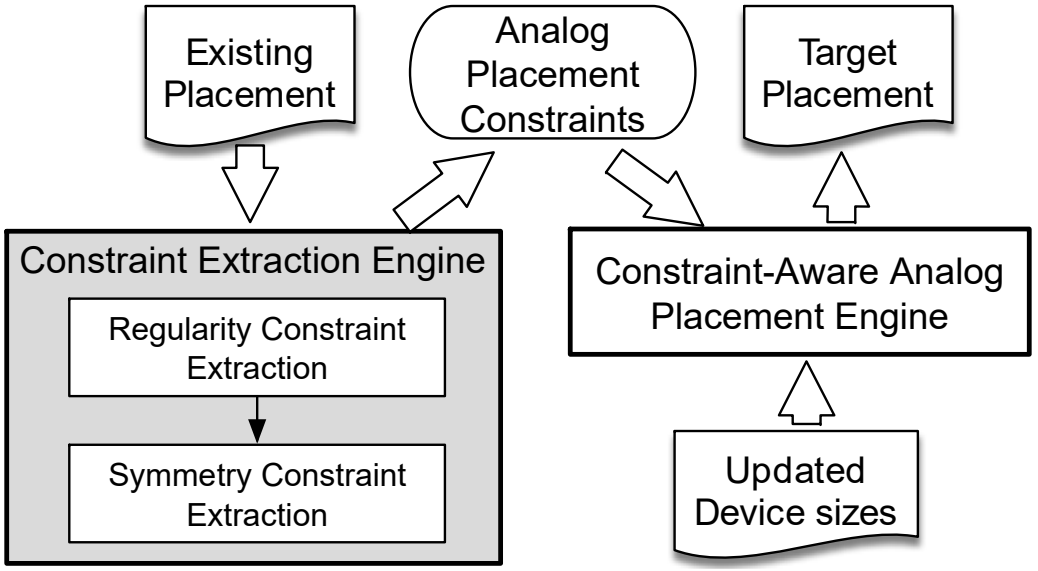


Sweep Line-Based Algorithm Example



Time complexity: $O(n^4)$

Constraint-Aware Placement



- Parallelized Mixed-Integer Linear Programming (MILP) formulation [B. Xu+, ISPD'17]
  - ✓ Objectives: min. area, etc.
  - ✓ Captures the constraints extracted, including symmetry and regularity

Regularity Constraints in MILP

- For every device d inside the kth regularity constraint:

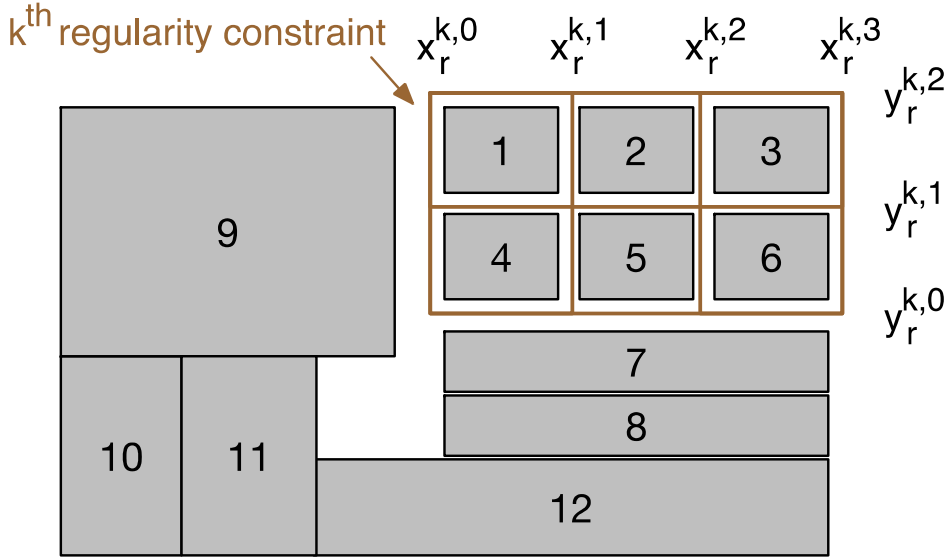
$$x_d \geq x_r^{k,j}, x_d \leq x_r^{k,j+1}, y_d \geq y_r^{k,i}, y_d \leq y_r^{k,i+1}, \forall d \in D_{i,j,k}$$

- For every device d' outside of the kth regularity constraint:

$$\begin{cases} x_{d'} + M_W(s_{d'}^k + t_{d'}^k) \geq x_r^{k,j^k} \\ x_{d'} + w_{d'} - M_W(1 + s_{d'}^k - t_{d'}^k) \leq x_r^{k,0} \\ y_{d'} + M_H(1 - s_{d'}^k + t_{d'}^k) \geq y_r^{k,i^k} \\ y_{d'} + h_{d'} - M_H(2 - s_{d'}^k - t_{d'}^k) \leq y_r^{k,0} \end{cases} \quad \forall d' \notin D_{i,j,k}$$

big-M method

[S. Sutanthavibul+, TCAD'91]



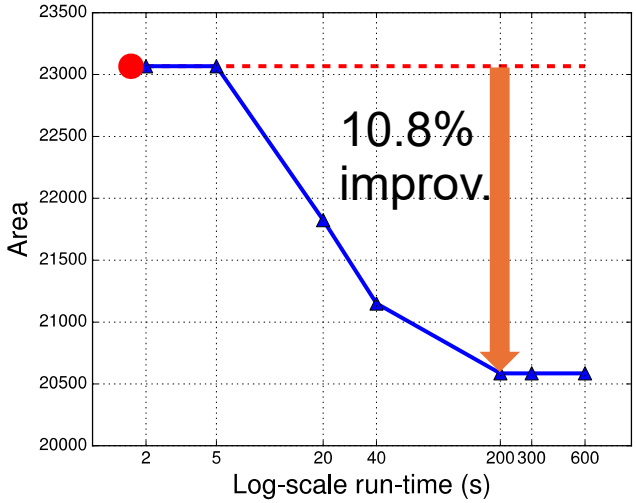
Experimental Results

- Implemented in C++ and all experiments are performed on a Linux machine with 3.4GHz CPU and 32GB memory
- To mimic layout retargeting, percentages of the size deviation are generated uniformly randomly in the range [-30%, +30%]
- Baseline [Z. Liu+, ASPDAC'10]
- Constraint extraction step takes < 0.01s for all benchmarks

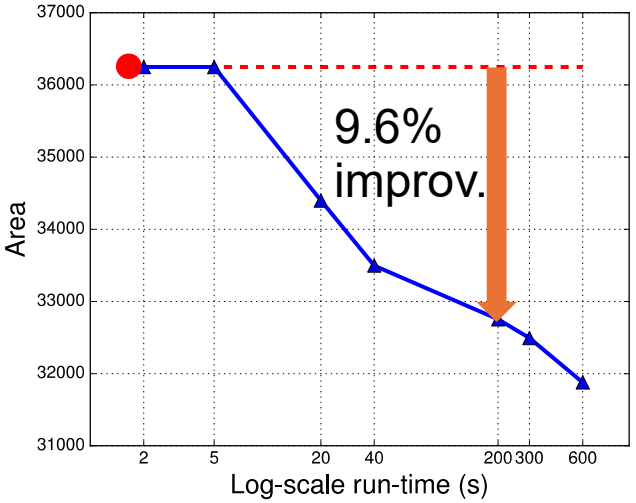
Benchmark	#Devices	#Row constraints	#column constraints	#Array constraints	#symmetry constraints
1	45	3	9	3	14
2	50	5	14	0	18
3	200	20	56	1	72

Experimental Results

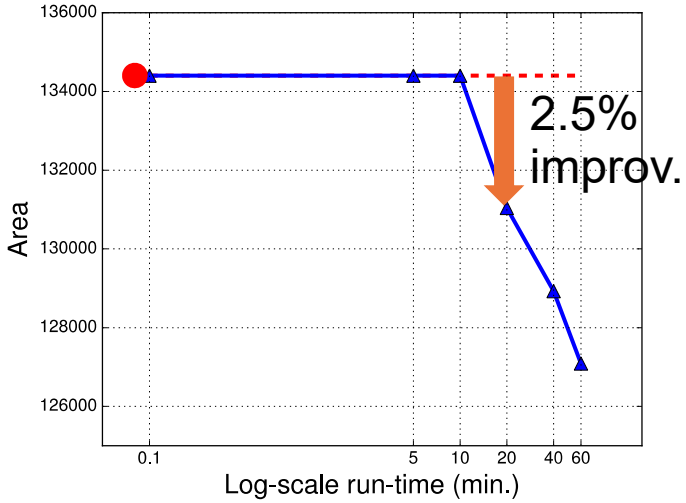
- Area v.s. layout retargeting run-time tradeoff
- 7.6% area improvement on average compared to [Z. Liu+, ASPDAC'10]



benchmark #1



benchmark #2



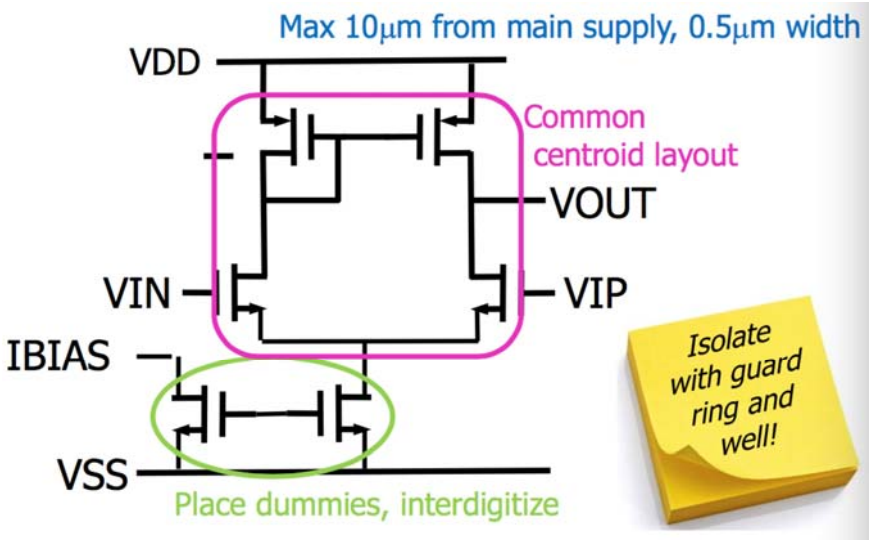
benchmark #3

[Z. Liu+, ASPDAC'10]

Ours

Summary

- A novel layout retargeting framework is proposed to preserve the symmetry and regularity constraints
- For the first time, an efficient sweep line-based algorithm is developed to extract all the regularity constraints in an analog placement
- On average, 7.6% placement area reduction compared with the conventional approach
- Future work:
  - ✓ Consider netlist info.
  - ✓ Extract more constraints



[A. Olofsson (DARPA), ISPD'18]

- Thanks!