Pioneer Research on Mathematical Models and Methods for Physical Design

A tribute to Prof. T. C. Hu

Chris Chu

Iowa State University

Advance Program

1997 International Symposium on Physical Design

Embassy Suites at Napa Valley, Napa, California

April 14–16, 1997

http://www.cs.virginia.edu/~ispd97/

The International Symposium on Physical Design provides a new and high-quality forum for the exchange of ideas and results in critical areas related to the physical design of VLSI systems. The Symposium is an outgrowth of the ACM/SIGDA Physical Design Workshops held during the years 1987-1996. Its scope includes all aspects of physical design, from interactions with behavior- and logic-level synthesis, to back-end performance analysis and verification.

This year's inaugural Symposium focuses on the challenges of high-performance deep-submicron design, as well as the necessary interactions between physical design and higher-level synthesis tasks. An outstanding slate of technical papers has been selected for oral and poster presentation. These developments are complemented by invited presentations that set forth the contexts and visions for key areas – process technology, system architecture, circuit design and design methodology – with an emphasis on their implications for relevant R&D in physical design. The Symposium concludes with a panel of leading experts who each present their unique perspectives as to the critical R&D needs of the field.

Monday, April 14

0830–0840 **Chairs' Welcome**

0840–1010 **Keynote Address**

- *Physical Design: Past and Future*, T. C. Hu (UCSD), E. S. Kuh (UCB)

1010–1030 **Break**

1230–1430 **Lunch** (Speaker)

- *The Quarter Micron Challenge: Integrating Physical and Logic Design*, R. Camposano (Synopsys)

1430–1600 **Session 2**
Synthesis and Layout

Chairs: R. Camposano (Synopsys)
C. Sechen (Washington)

- *Timing Driven Placement in Interaction with Netlist Transformations*, G. Stenz, B. R. Riess, B. Rohfleisch, F. M. Johannes (TU-Munich)
- *Regular Layout Generation of Logically Optimized Datapaths*, R.X.T. Nijssen, C.A.J. van Eijk (TU-Eindhoven)
- *Minimizing Interconnect Energy Through Integrated Low-Power Placement and Combinational Logic Synthesis*, G. Holt, A. Tyagi (Iowa State)

1600–1630 **Break**

1630–1830 **Session 3 (Invited)**
Contexts

- *Design Technology Trends Based on NTRS Evolution*, P. Verhofstadt, C. D'Angelo (SRC)
- *Microprocessor Architecture, Circuit, and Physical Design Trends*, R. Panwar (Sun)

1900–2100 **Dinner** (Speaker)

thography and Dimensional Trends for Future ocesses – Implications for Physical Design, K. Vasudev (Sematech)

PHYSICAL DESIGN: MATHEMATICAL MODELS AND METHODS
KEYNOTE ADDRESS

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In mathematical programming terms, we have a multi-objective or several objective functions. One way to handle multiple objectives is to use a weighted objective function with the weighting factor proportional to the importance of the term (say, speed or area). During the optimization process, if the speed of the chip is fast enough, we can delete speed as an objective and maintain speed as a constraint.

Second, we usually do not have the time to design every cell in a tailor-made fashion; it is much cheaper and less error-prone if we build the design from a cell library. The situation is similar to building a house where windows have standard sizes. In other words, we restrict our variables to have only limited, fixed values. In the extreme case, we want the variables x_j to be zero or one. Or, we may want all solutions to be positive integers and not arbitrary real values. In design terms, we need "modular" designs. In

to find the route to the destination of minimum total cost.

The cost associated with the block or the channel is the *shadow price* of that channel. The shadow price is zero when the channel is empty, and keeps changing as we gradually assign nets in the channel. However, the correct price to be assigned to a given channel does not depend only on the number of nets in that channel — it also depends on the "traffic" in the neighboring channels, and indeed the neighboring channels of neighboring channels.

In LP we have a square matrix B reflecting the current routing, while the shadow price is obtained by multiplying the current cost by the inverse matrix B^{-1}. The inverse matrix B^{-1} not only gives the shadow price but also records what we have done.

2.2. Column Generating Techniques

M. Weisel (Intel)

- *A Roadmap of CAD Tool Changes for Sub-Micron Interconnect Problems*, L. Scheffer (Cadence)
- *C5M - A Control Logic Layout Synthesis System for High-performance Microprocessors*, J. Burns, J. Feldman (IBM)
- *A VLSI Artwork Legalization Technique Based on a New Criterion of Minimum Layout Perturbation*, F.-L. Heng, Z. Chen, G. E. Tellez (IBM)

1500–1545 **Session 7**
Poster Presentations

Chairs: G. Robins (Virginia)
J. D. Cho (SungKyunKwan)

- *A Pseudo-Hierarchical Methodology for High Performance Microprocessor Design*, A. Bertolet, K. Carpenter, K. Carrig, A. Chu, A. Dean, F. Ferraiolo, S. Kenyon, D. Phan, J. Petrovick, G. Rodgers, D. Willmott (IBM); T. Bairley, T. Decker, V. Girardi, Y. Lapid, M. Murphy, P. A. Scott, R. Weiss (Cadence)
- *Concurrent Transistor Sizing and Buffer Insertion by Considering Cost-Delay Tradeoffs*, J. Kim, C. Bamji (Cadence); Y. Jiang, S. Sapatnekar (Iowa State)
- *Towards a New Benchmarking Paradigm in EDA*, N. Kapur, D. Ghosh, F. Brglez (NCSU)
- *How Good are Slicing Floorplans?*, F. Y. Young, D. F. Wong (UT-Austin)
- *Slicibility of Rectangular Graphs and Floorplan Optimization*, P. DasGupta, S. Sur-kolay (Indian Institute of Management)
- *Power Optimization for FPGA Look-Up Tables*, M. J. Alexander (Washington State)
- *A Matrix Synthesis Approach to Thermal Placement*, C. C.-N Chu, D. F. Wong (UT-Austin)
- *Preserving HDL Synthesis Hierarchy for Cell Placement*, Y.-W. Tsay, W.-J. Fang, A. C.-H. Wu

tion of High Speed VLSI Buffers, D. Zhou, X. Y. Liu, X. L. Wang (UNC-Charlotte)

- *Closed Form Solution to Simultaneous Buffer Insertion/Sizing and Wire Sizing*, C. C.-N. Chu, D. F. Wong (UT-Austin)

1000–1030 **Break**

1030–1230 **Session 10 (Invited)**
Design Methodology Futures

- *Chip Hierarchical Design System (CHDS): A Foundation for Timing-Driven Physical Design into the 21st Century*, R. G. Bushroe (Sematech/HP), S. DasGupta (IBM) and R. Steele (Sematech/Intel)
- *Physical Design 2010: Back to the Future?*, A. R. Newton (UCB)

1230–1430 **Lunch** (Speaker)

- *Physical Design Realities for Digital's StrongARM and Alpha Microprocessors*, W. J. Grundmann (DEC)

1430–1700 **Session 11 (Invited)**
Core Directions (or, Do The Right Thing)

- *Physical Design Challenges of Performance*, D. P. LaPotin (IBM Austin Research Lab)
- **Panel:** Physical Design R&D: What's Missing?

  Moderator: G. Smith (Dataquest)
  W. W.-M. Dai (UCSC)
  E. Hsieh (Avant!)
  M. Hunt (Cadence)
  K. Keutzer (Synopsys)
  D. P. LaPotin (IBM Austin Research Lab)
  N. Sherwani (Intel Hillsboro)

1700 **Symposium Closes**

A Confession …..

- A Thermal Synthesis Approach to Thermal Placement
  - Unrealistic thermal model
  - Restrictive array-based layout style
  - Randomly generated thermal numbers
  - ….
- Closed Form Solution to Simultaneous Buffer Insertion/Sizing and Wire Sizing
  - Simplistic Elmore delay model
  - Continuous wire width and gate size assumption
  - Ignoring bounds on wire width and gate size
  - ….

Why were they accepted?

- A Thermal Synthesis Approach to Thermal Placement
  - 5 Theorems, 3 Lemmas

- Closed Form Solution to Simultaneous Buffer Insertion/Sizing and Wire Sizing
  - 3 Theorems, 10 Lemmas

"We don't prove very much these days."
-- Andrew Kahng (3/26/2018)

Learn from Prof. Hu

PHYSICAL DESIGN: MATHEMATICAL MODELS AND METHODS
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Generalization of Max-Flow Min-Cut Theorem

- T. C. Hu, "Multi-commodity network flows," Operations Research, 11(3):344–360, 1963.

Theorem 1. (Max Bi-Flows Min-Cut Theorem)

Two flows F (1; 1′) and F (2; 2′) are feasible if and only if (1), (2), (3) below are all satisfied:

$$f(1; 1') \le c(1; 1') \qquad (1)$$

$$f(2; 2') \le c(2; 2') \qquad (2)$$

$$f(1; 1') + f(2; 2') \le c(1, 2; 1', 2') \qquad (3)$$

The maximum sum of the two flows is equal to the minimum-cut capacity of all cuts separating the two pairs of nodes; i.e., $\max[f(1; 1') + f(2; 2')] = \min[c(1 - 2; 1' - 2'), c(1 - 2'; 1' - 2)]$.

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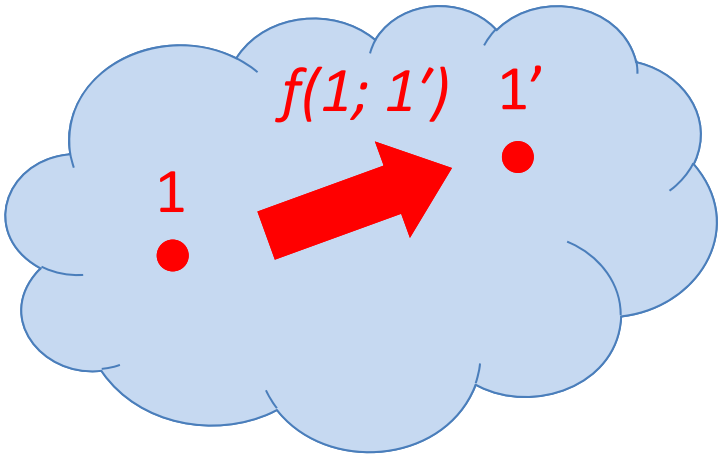

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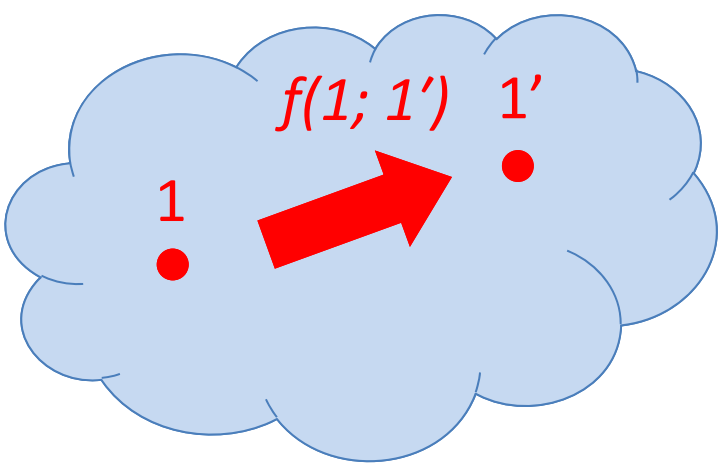

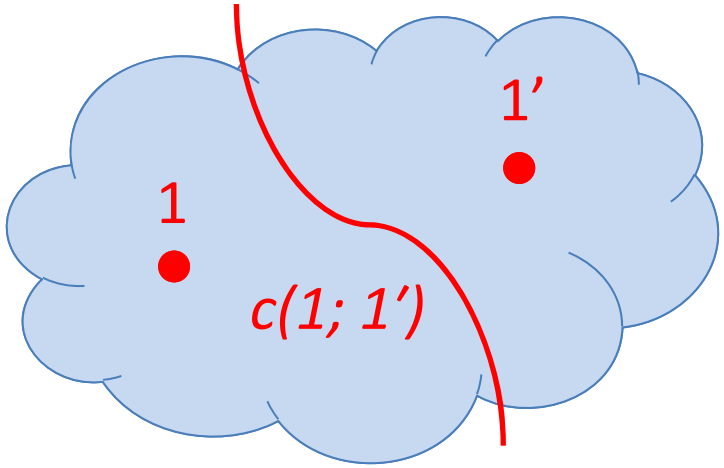

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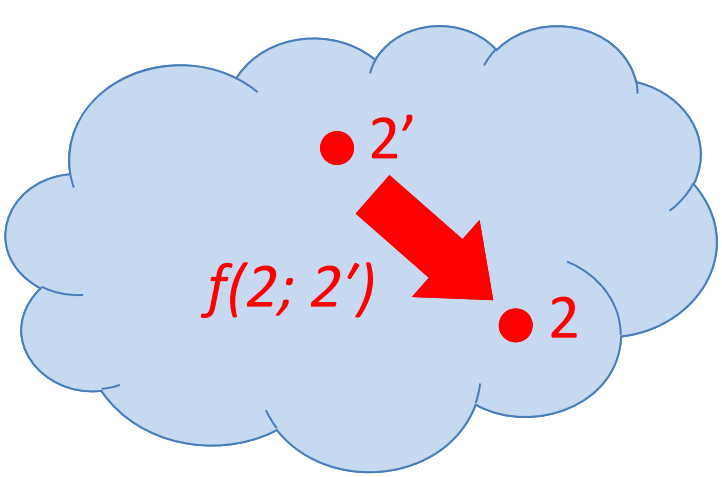

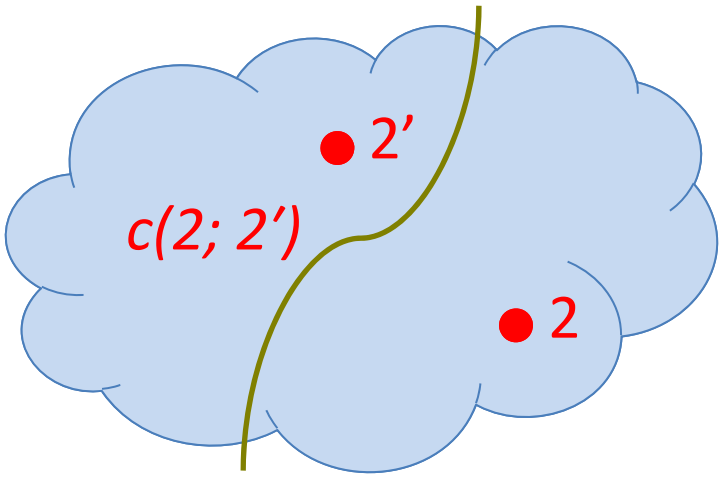

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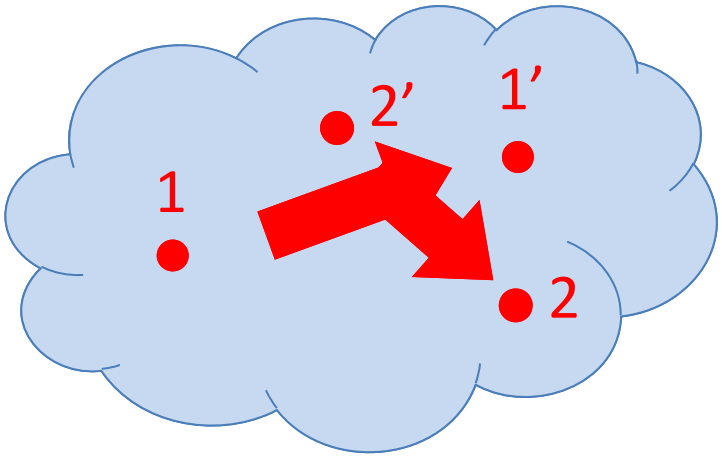

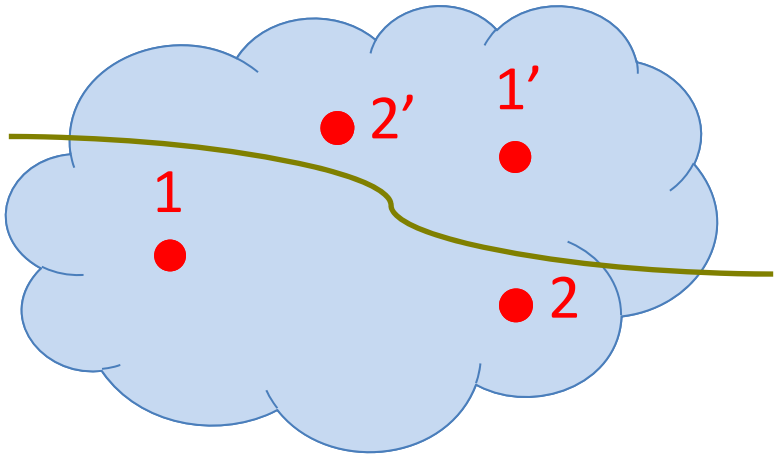

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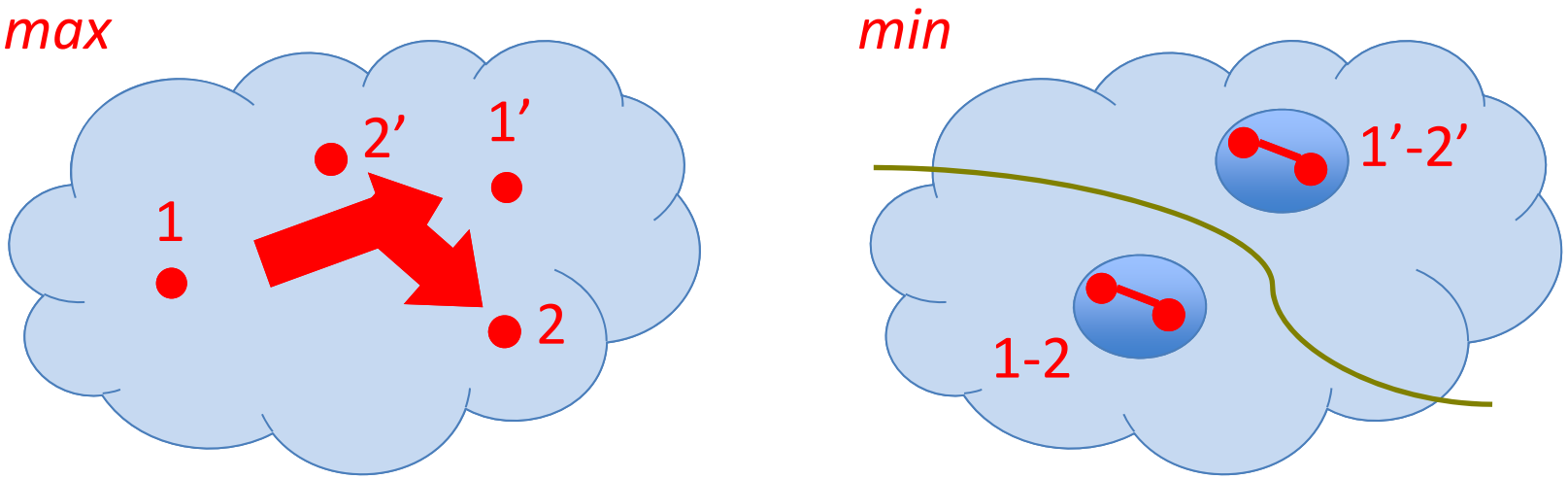
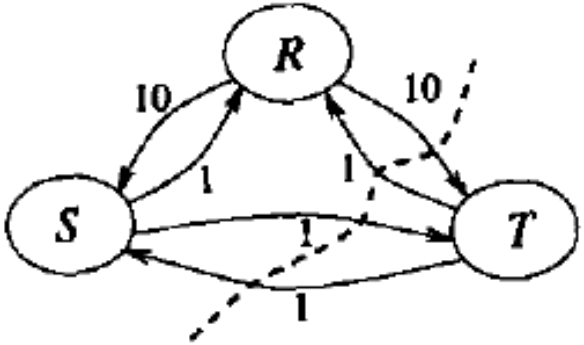
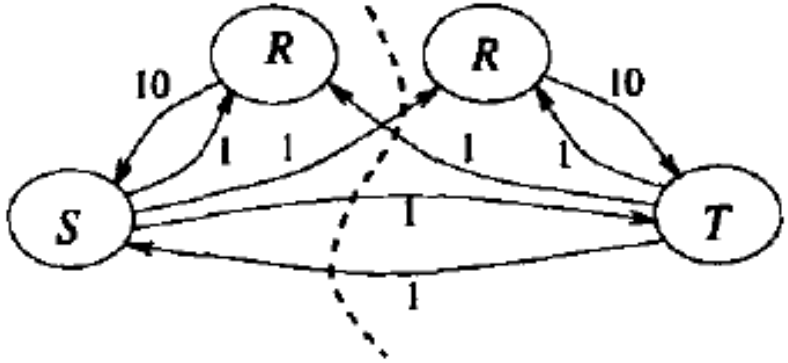


Replication Cut

- Lung-Tien Liu, Ming-Ter Kuo, Chung-Kuan Cheng, and T. C. Hu, “A replication cut for two-way partitioning”. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 14(5):623–630, May 1995.

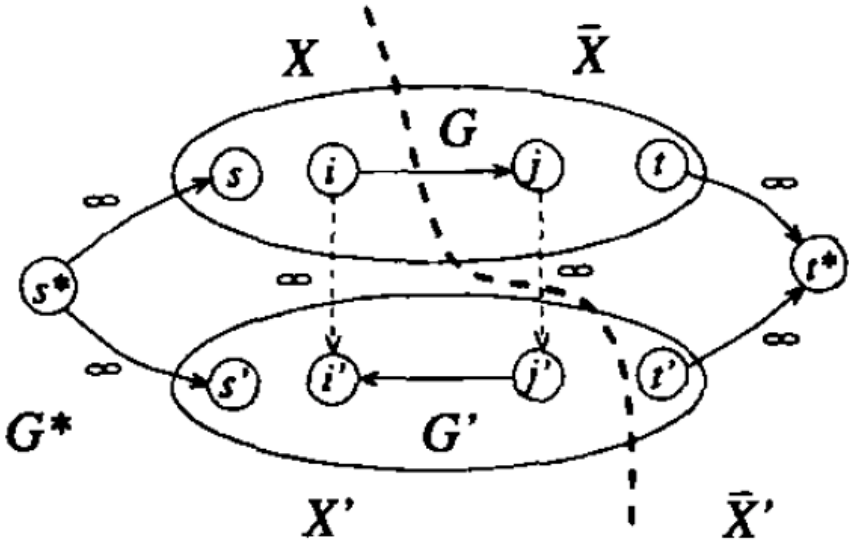


Min-cut



Min-cut with cell replication

Maximum Flow based Solution



- 1997 IEEE Circuit and System Society Best Paper Award

Take-Home Messages

- Paper reviewers:
  - *Don't reject my papers* *just because they don't consider all practical issues.*
  - Reject if they do not have insightful, inspiring ideas.
- Researchers:
  - Pursue long-lasting impact.
  - Both theoretical work and practical work are valuable.
- Students:
  - Look up to Prof. Hu.
- Prof. Hu:

Congratulations and Thank you!