The Pressing Need for Electromigration-Aware Physical Design

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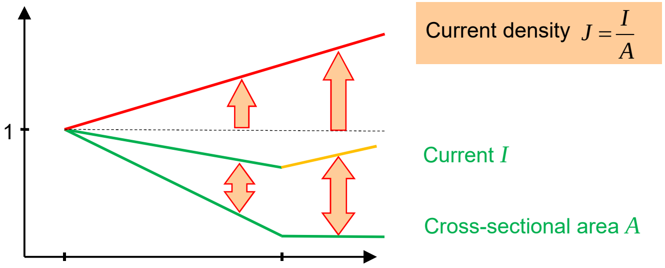
ITRS

Year	2018	2020	2022	2024	2026	2028	
Gate length (nm)	12.8	10.65	8.87	7.39	6.16	5.13	↓
On-chip local clock frequency (GHz)	6.69	7.24	7.83	8.47	9.16	9.91	↑
DC equivalent maximum current (μA)	6.92	4.41	2.33	2.98	3.56	4.24	↓ ↑
Metal 1 properties							
Cross-sectional area (nm²)	302.4	170.1	79.2	79.2	79.2	79.2	↓ →



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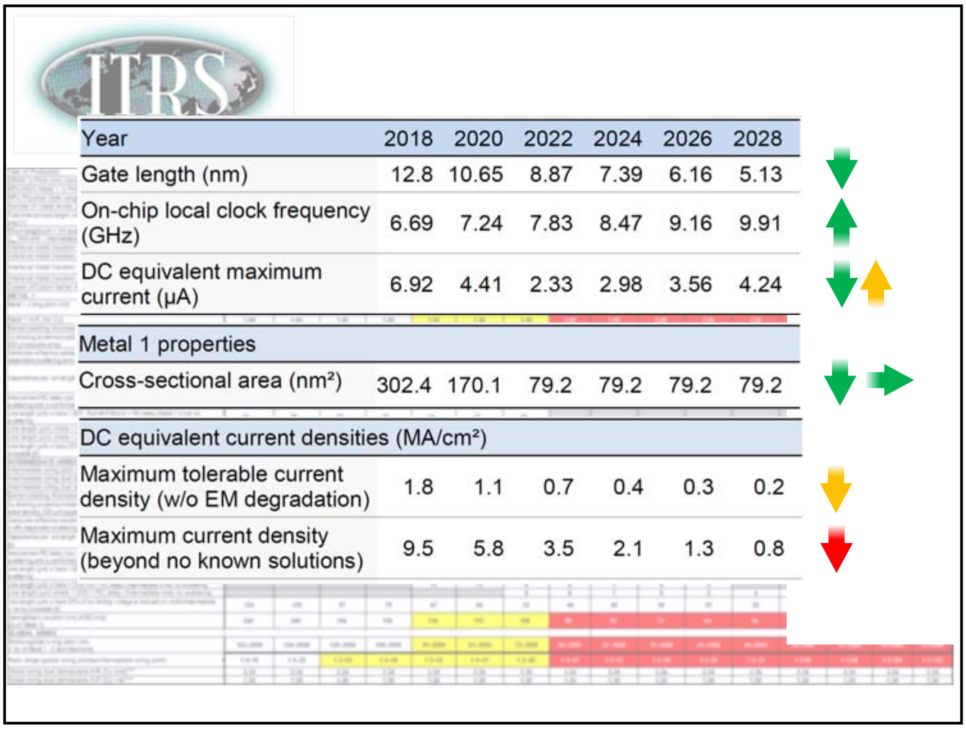

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Metal 1 properties							
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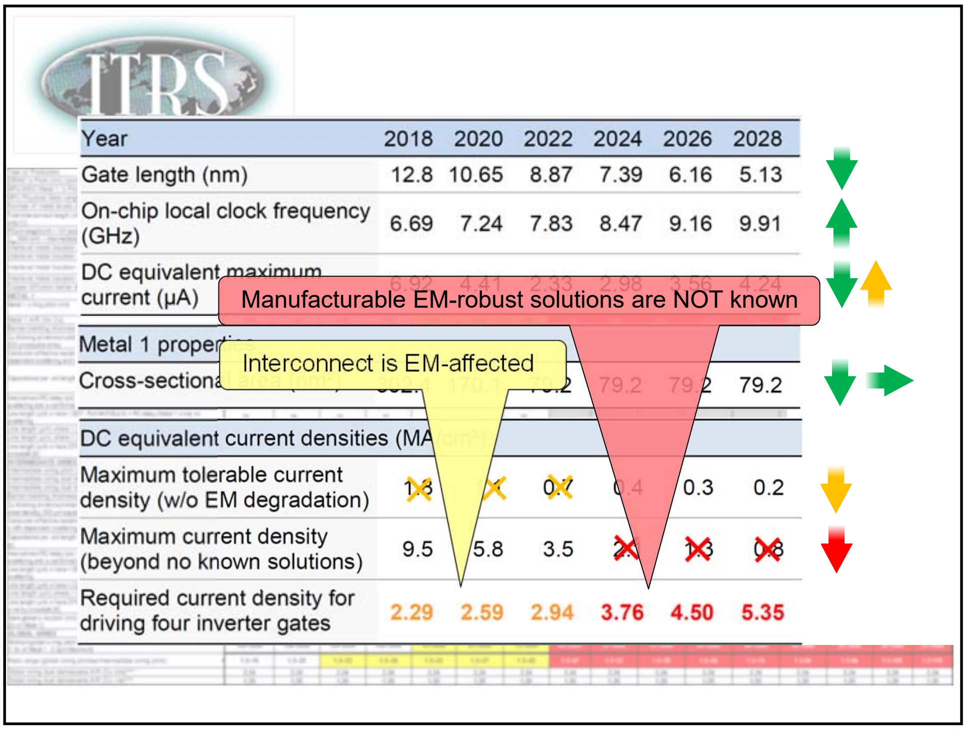
DC equivalent current densities (MA/cm²)							
Maximum tolerable current density (w/o EM degradation)	1.8	1.1	0.7	0.4	0.3	0.2	↓
Maximum current density (beyond no known solutions)	9.5	5.8	3.5	2.1	1.3	0.8	↓



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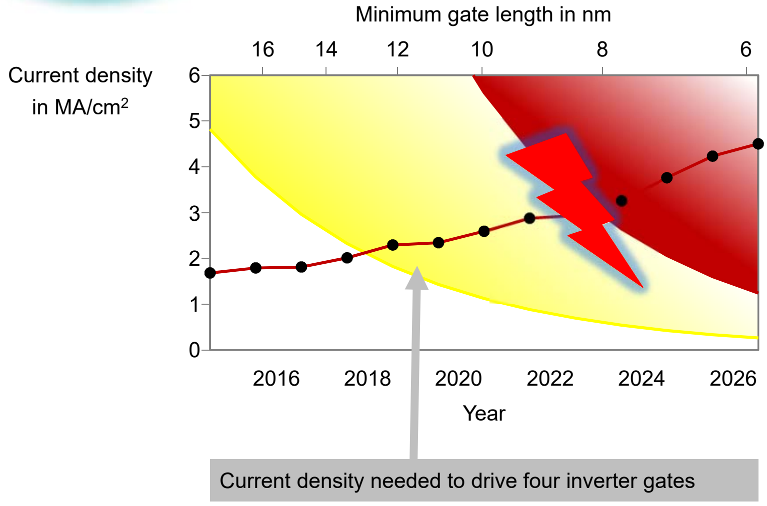
DC equivalent current densities (MA/cm²)							
Maximum tolerable current density (w/o EM degradation)	~~1.8~~	~~1.1~~	~~0.7~~	0.4	0.3	0.2	↓
Maximum current density (beyond no known solutions)	9.5	5.8	3.5	~~2.1~~	~~1.3~~	~~0.8~~	↓
Required current density for driving four inverter gates	2.29	2.59	2.94	3.76	4.50	5.35	

Manufacturable EM-robust solutions are NOT known

Interconnect is EM-affected



Current density needed to drive four inverter gates

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1 Introduction to Electromigration (EM)

2 Mitigating EM in Physical Design – What are Today's Options?

3 Outlook – What to Do in the "Red Area"?

4 Summary

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Introduction: Electromigration

Electromigration (EM):

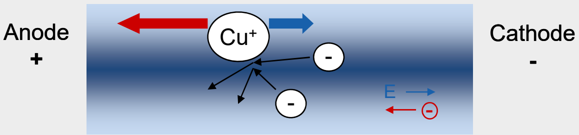
Electromigration is the forced movement of metal ions due to an electric field

$F_{total} = F_{direct} + F_{wind}$

Direct action of electric field on metal ions

<<

Force on metal ions resulting from momentum transfer from the conduction electrons



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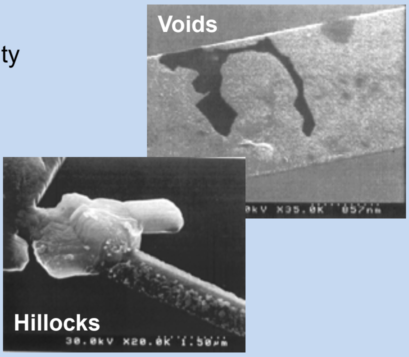
Introduction: Electromigration

⇒ Metal atoms (ions) travel towards the positive end of the conductor while vacancies move towards the negative end

Effects of electromigration in metal interconnects:

- Atomic depletion (voids):
  → Slow reduction in connectivity
  → Interconnect failure
- Atomic deposition (hillocks, whiskers):
  → Short-cuts



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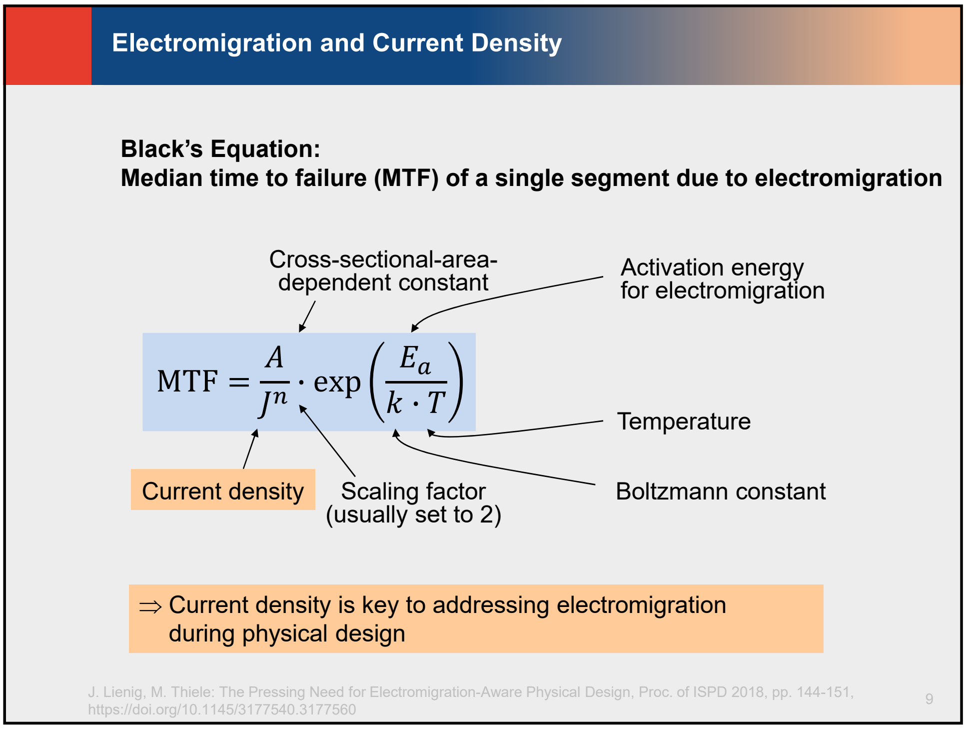

Electromigration and Current Density

Black's Equation:
Median time to failure (MTF) of a single segment due to electromigration

$$\mathrm{MTF} = \frac{A}{J^n} \cdot \exp\left(\frac{E_a}{k \cdot T}\right)$$

⇒ Current density is key to addressing electromigration during physical design

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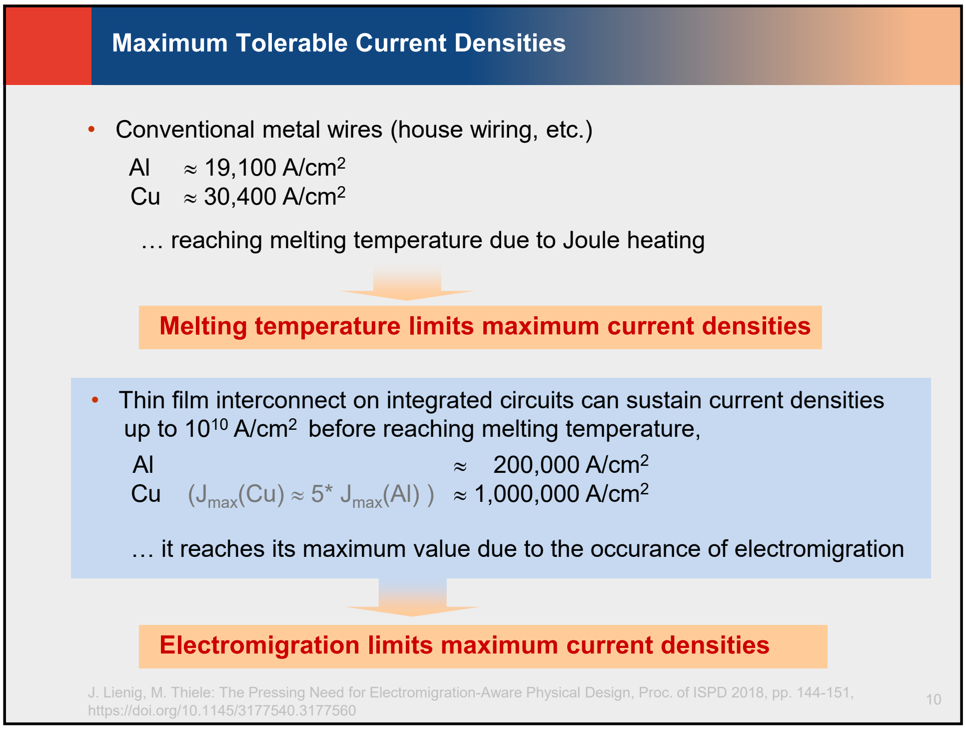

Maximum Tolerable Current Densities

- Conventional metal wires (house wiring, etc.)

  Al ≈ 19,100 A/cm^2
  Cu ≈ 30,400 A/cm^2

  … reaching melting temperature due to Joule heating

Melting temperature limits maximum current densities

- Thin film interconnect on integrated circuits can sustain current densities up to 10^{10} A/cm^2 before reaching melting temperature,

  Al ≈ 200,000 A/cm^2
  Cu (J_{max}(Cu) ≈ 5* J_{max}(Al)) ≈ 1,000,000 A/cm^2

  … it reaches its maximum value due to the occurance of electromigration

Electromigration limits maximum current densities

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Maximum Tolerable Current Densities

- Rule of Thumb for Copper IC Interconnects

Electromigration to be considered	≈ 10,000 - 100,000	A/cm^2
Effects visible	≈ 500,000	A/cm^2
Rapid destruction	≈ 30,000,000	A/cm^2

(25°C, Source: AMD Saxony)

Electromigration limits maximum current densities

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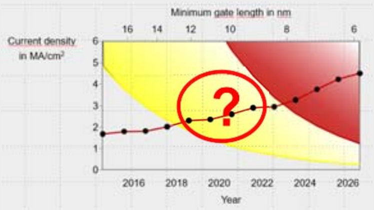

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Mitigating EM in Physical Design – What are Today's Options?

Local current density	**Wire widths, double/multiple vias**
Surface diffusion in Cu	**Surface coating, metal capping**
Bamboo effect	**Wire widths**
Short-length effects	**Segment lengths**
Impact of voids	**Via-above/via-below configurations**
Reservoir effect	**(Metal-via) overlaps, multiple vias**
Damage-healing (self-healing) effect	**Frequency of the current**

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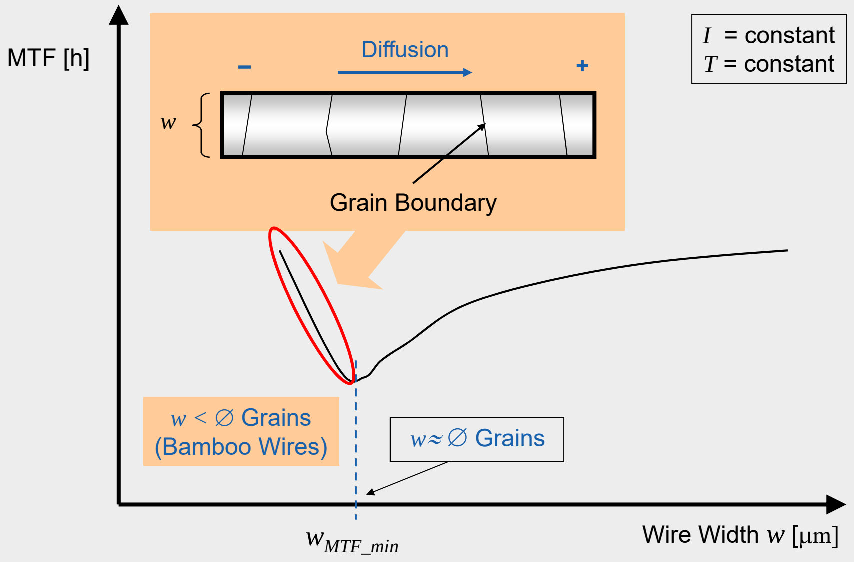
Bamboo Effect



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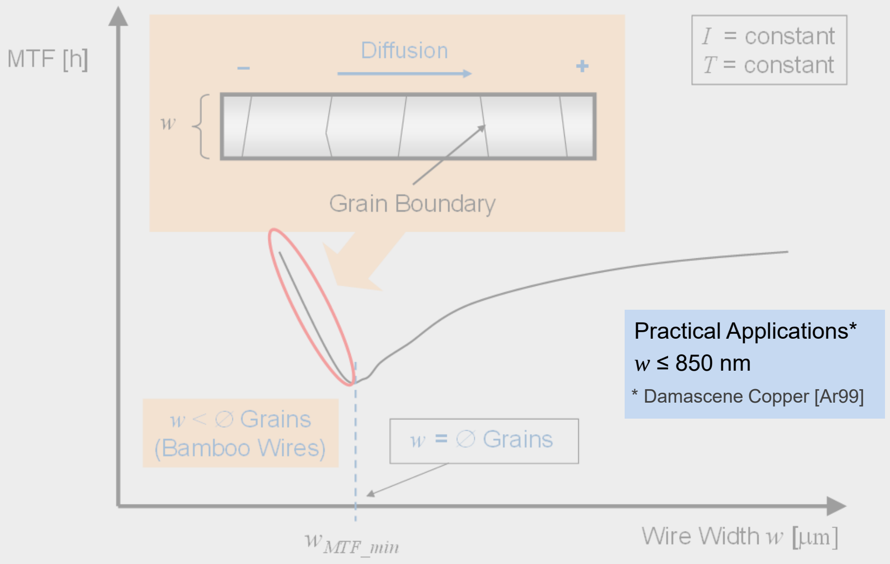
Bamboo Effect



Practical Applications*
$w \le 850$ nm

* Damascene Copper [Ar99]

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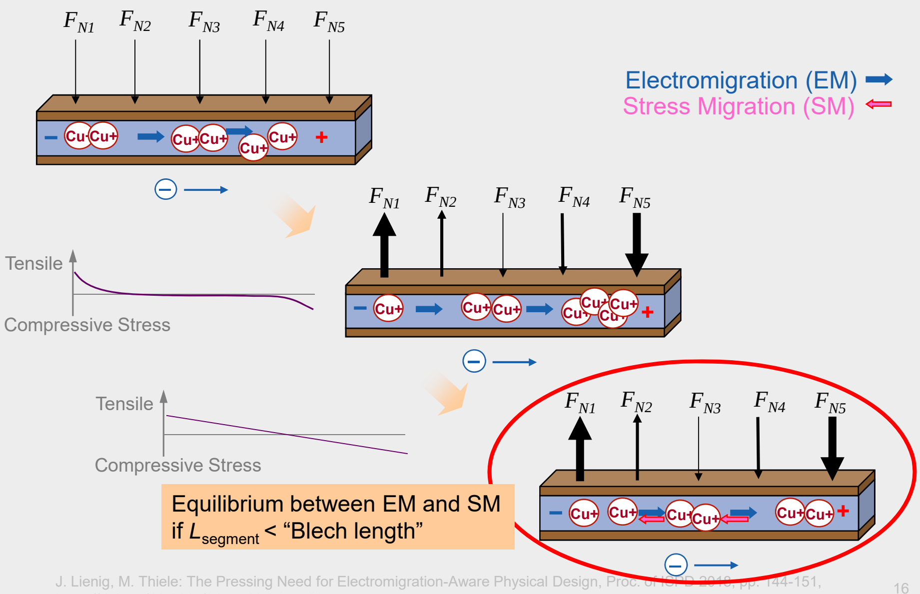
Short-Length Effects: (1) Blech Immortality Condition



Electromigration (EM) ➡
Stress Migration (SM) ⇦

Equilibrium between EM and SM if $L_{segment}$ < "Blech length"

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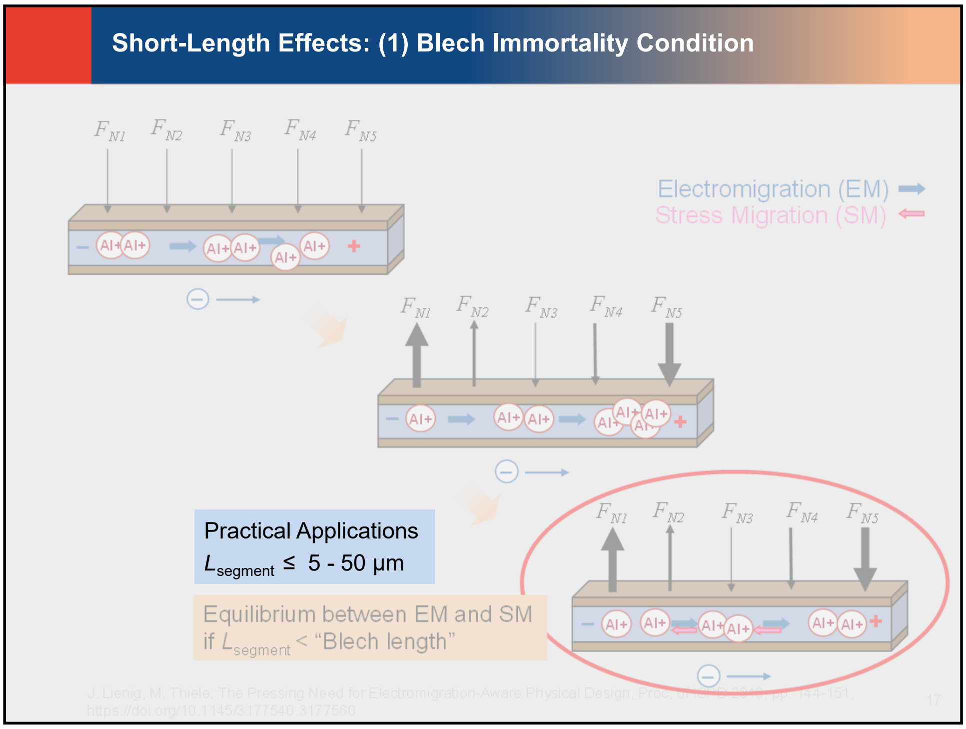

Short-Length Effects: (1) Blech Immortality Condition

Practical Applications
$L_{segment} \leq$ 5 - 50 µm

Equilibrium between EM and SM
if $L_{segment}$ < "Blech length"

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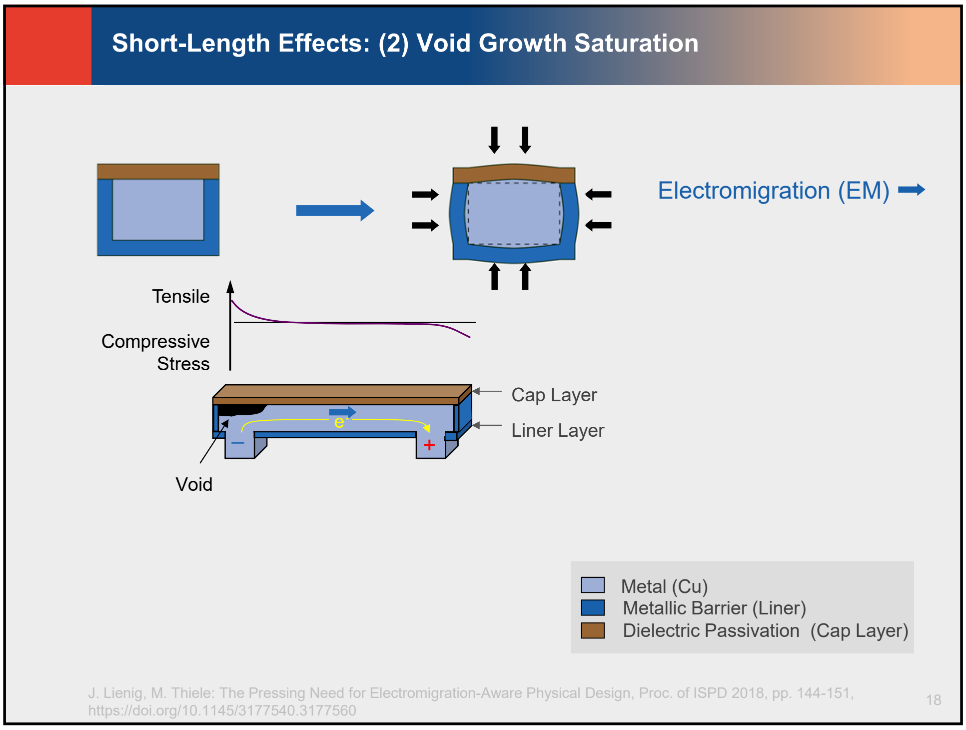

Short-Length Effects: (2) Void Growth Saturation

▨ Metal (Cu)
▨ Metallic Barrier (Liner)
▨ Dielectric Passivation (Cap Layer)

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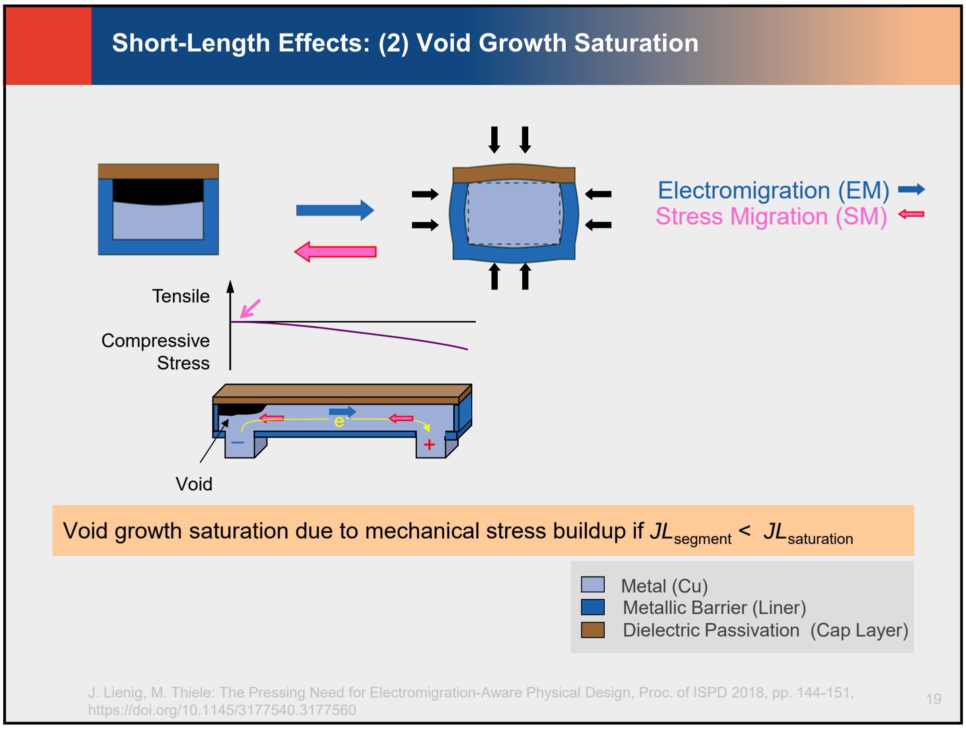

Short-Length Effects: (2) Void Growth Saturation

Void growth saturation due to mechanical stress buildup if $JL_{segment} < JL_{saturation}$

- ▨ Metal (Cu)
- 🟦 Metallic Barrier (Liner)
- 🟫 Dielectric Passivation (Cap Layer)

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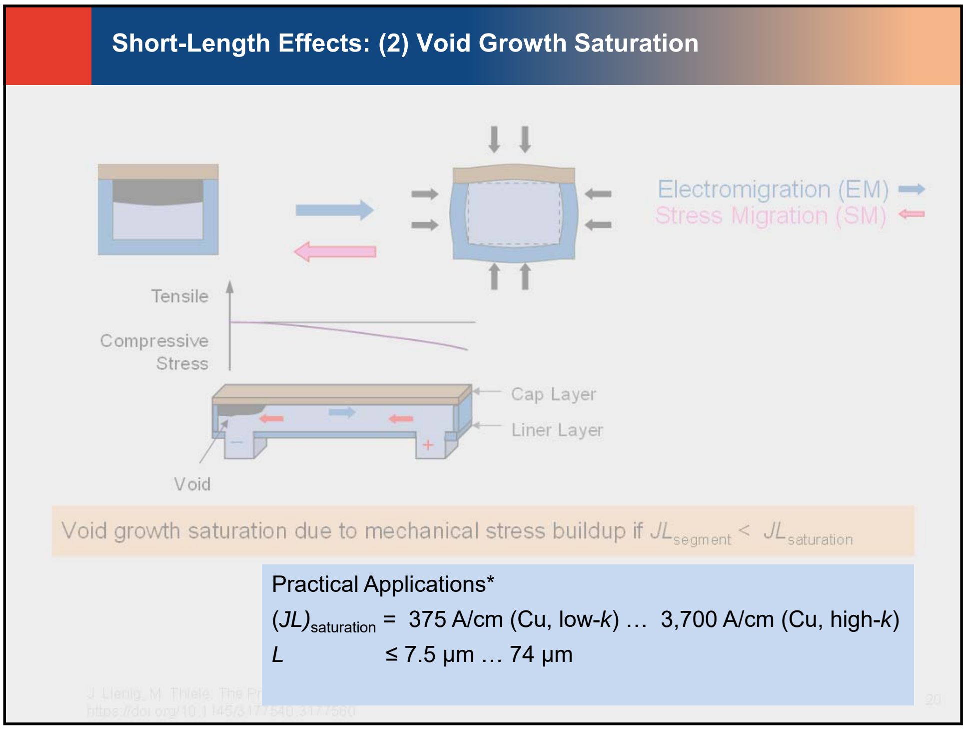

Short-Length Effects: (2) Void Growth Saturation

Void growth saturation due to mechanical stress buildup if $JL_{segment} < JL_{saturation}$

Practical Applications*

$(JL)_{saturation}$ = 375 A/cm (Cu, low-k) … 3,700 A/cm (Cu, high-k)

L ≤ 7.5 µm … 74 µm

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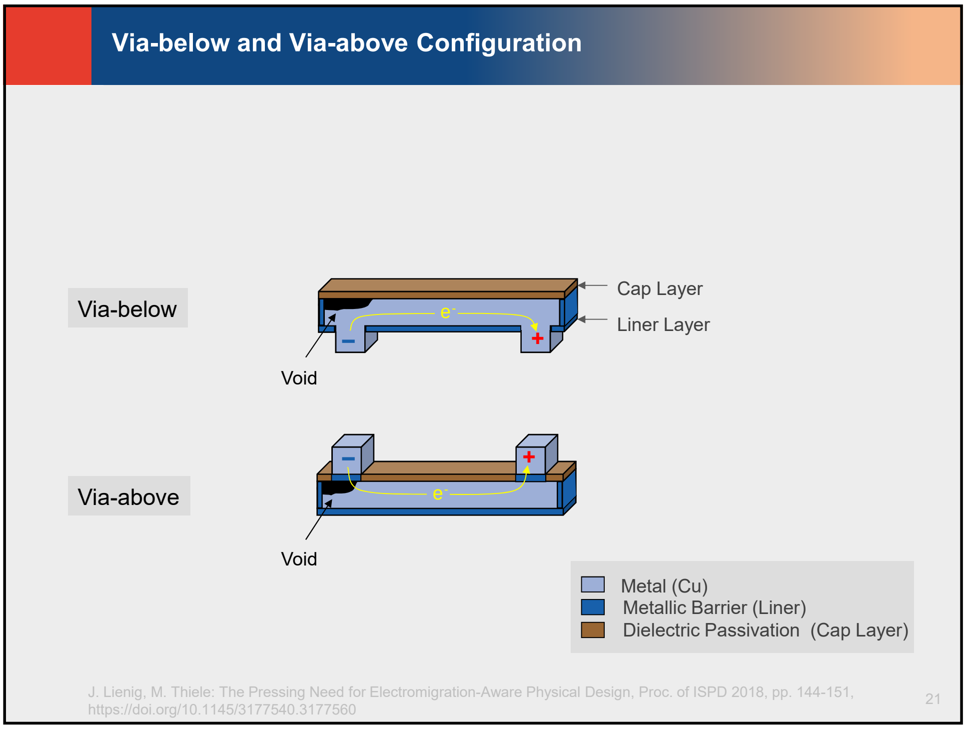

Via-below and Via-above Configuration

Via-below

Cap Layer

Liner Layer

Void

Via-above

Void

▨ Metal (Cu)
🟦 Metallic Barrier (Liner)
🟫 Dielectric Passivation (Cap Layer)

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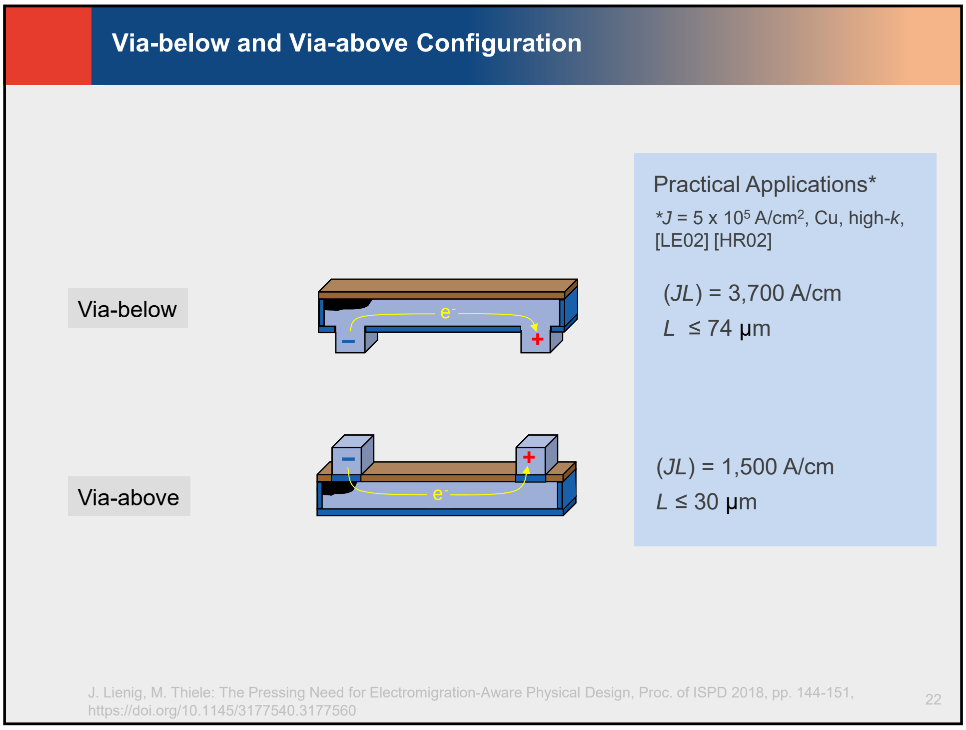

Via-below and Via-above Configuration

Via-below

Via-above

Practical Applications*

*$J = 5 \times 10^5$ A/cm^2, Cu, high-k, [LE02] [HR02]

$(JL) = 3{,}700$ A/cm

$L \leq 74$ µm

$(JL) = 1{,}500$ A/cm

$L \leq 30$ µm

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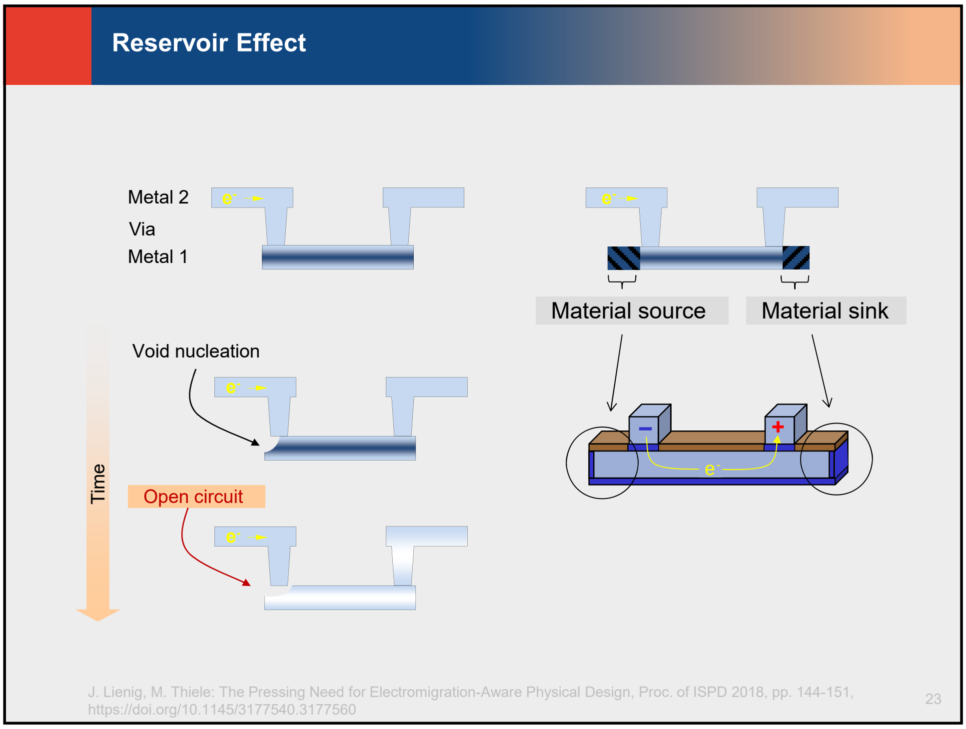

Reservoir Effect

Metal 2

Via

Metal 1

Void nucleation

Open circuit

Time

Material source

Material sink

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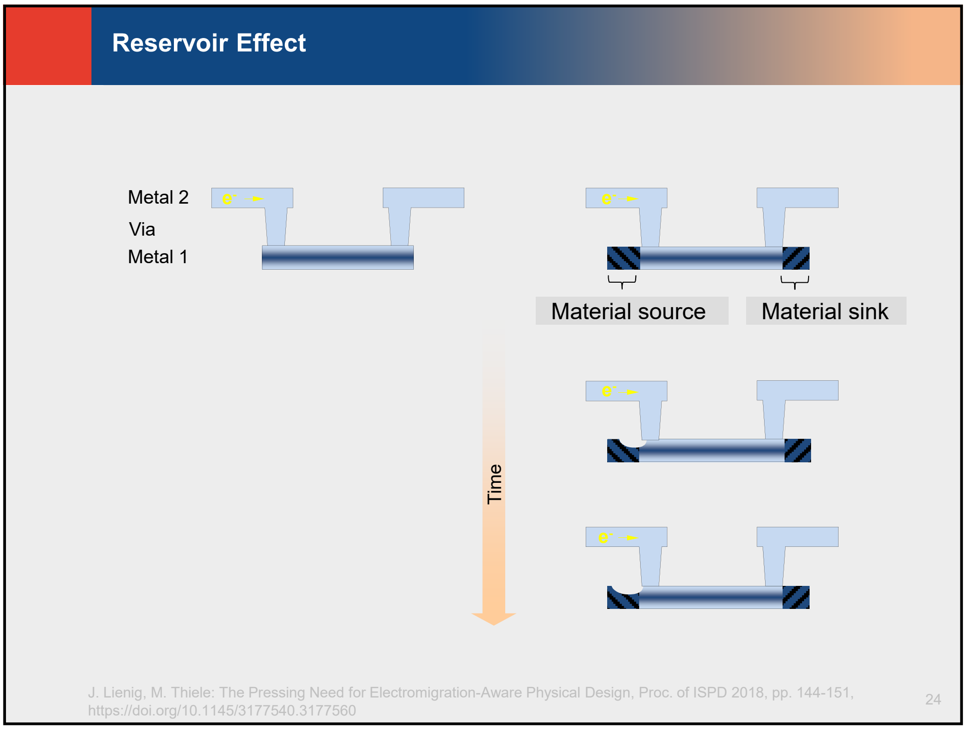

Reservoir Effect

Metal 2

Via

Metal 1

Material source

Material sink

Time

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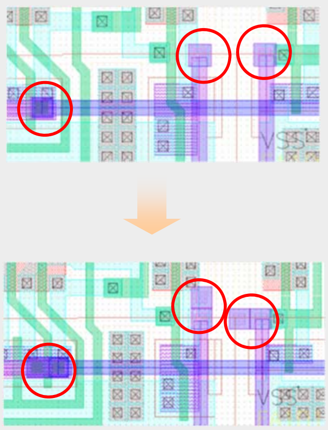
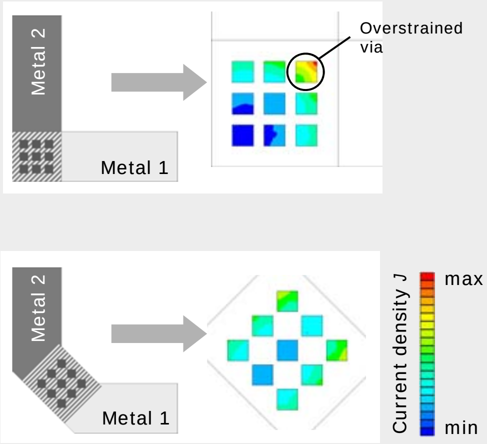
Double/Multiple Vias



http://www.ee.ncu.edu.tw/~cad_contest/Problems/95/PB2/2007_B2.pdf



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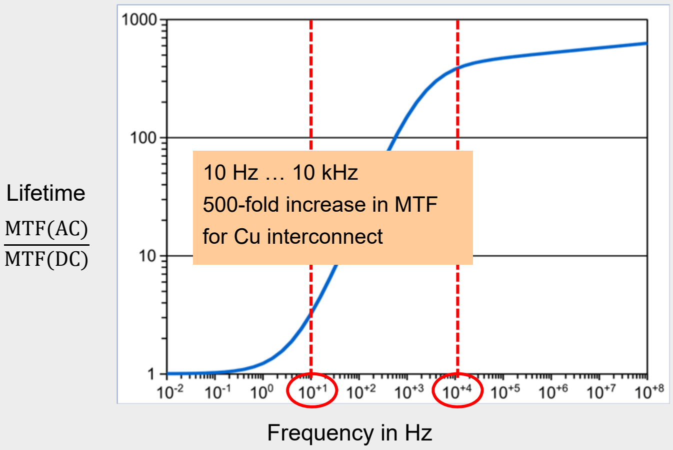
Self-Healing Effect



10 Hz … 10 kHz
500-fold increase in MTF
for Cu interconnect

Tao, J.; Cheung, N.; Hu, C.: Metal Electromigration Damage Healing under Bidirectional Current Stress, *Electron Device Letters, IEEE*, vol. 14, no. 12, 554–556, 1993

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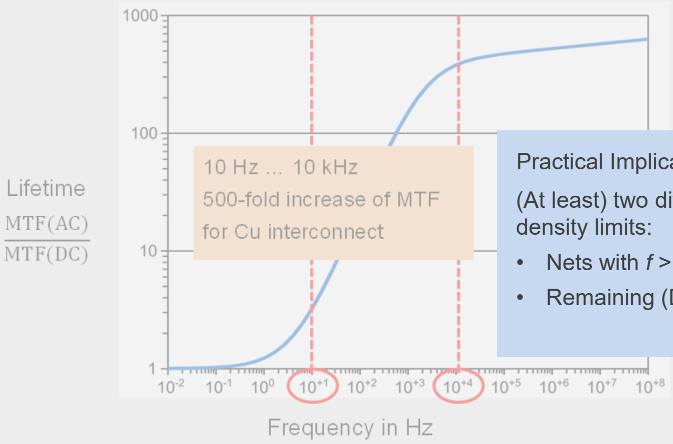

10 Hz … 10 kHz
500-fold increase of MTF
for Cu interconnect

Practical Implication

(At least) two different current density limits:

- Nets with *f* > 10 kHz
- Remaining (DC) nets

Tao, J.; Cheung, N.; Hu, C.: Metal Electromigration Damage Healing under Bidirectional Current Stress, Electron Device Letters, IEEE, vol. 14, no. 12, 554–556, 1993

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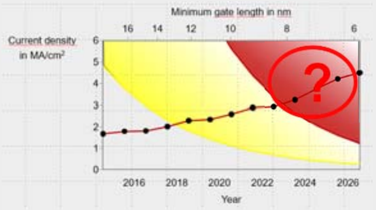

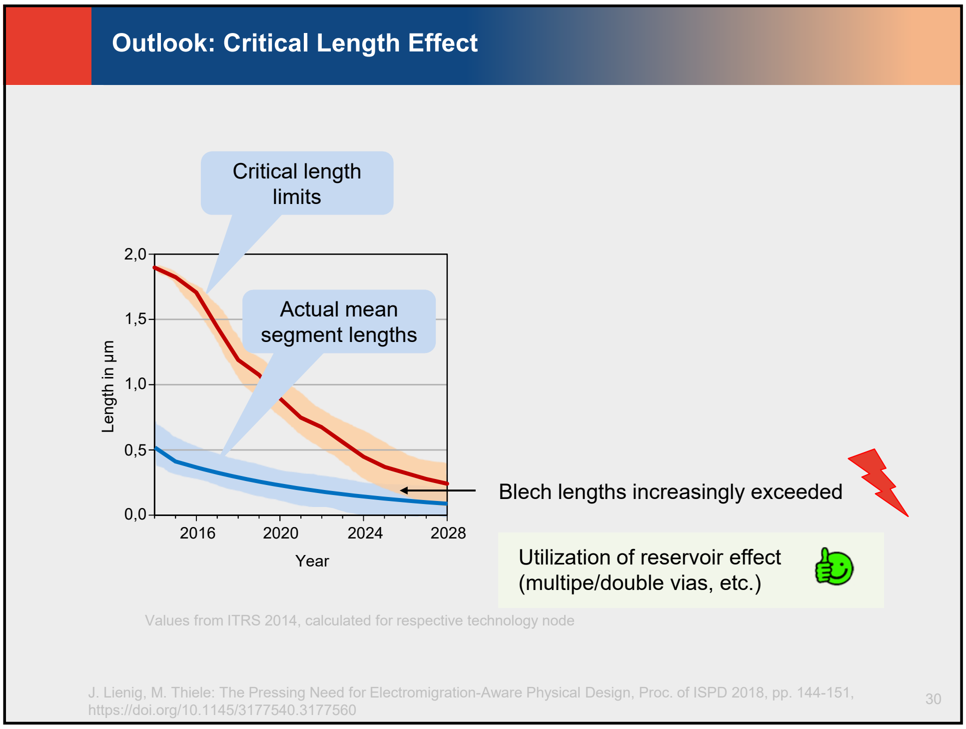

Outlook: Critical Length Effect

Critical length limits

Actual mean segment lengths

Blech lengths increasingly exceeded

Utilization of reservoir effect (multipe/double vias, etc.)

Values from ITRS 2014, calculated for respective technology node

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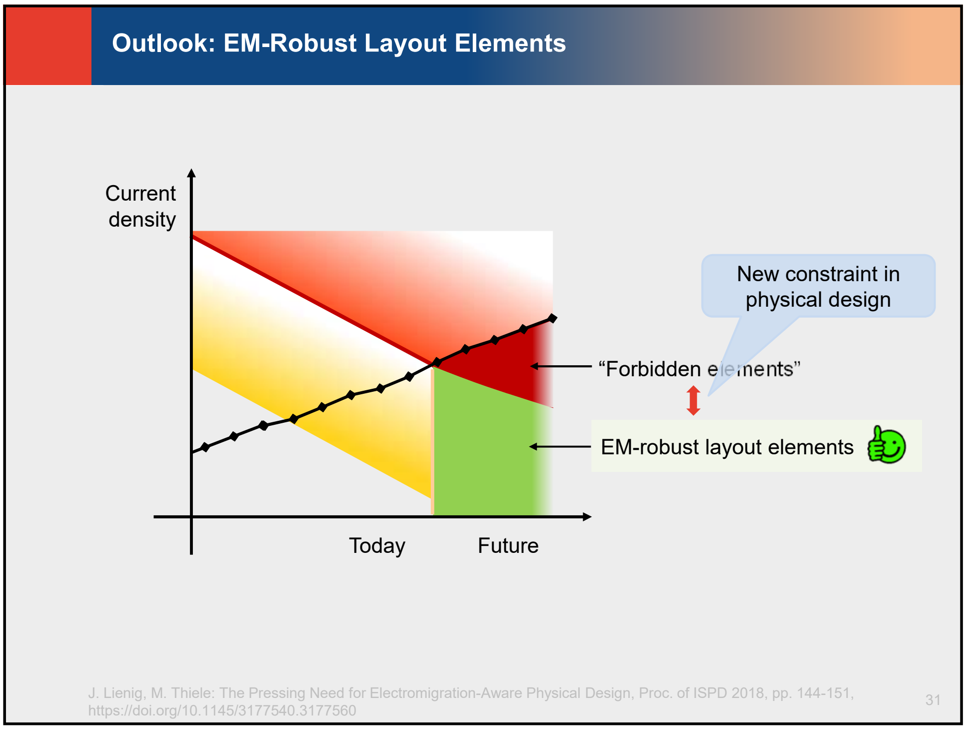

Outlook: EM-Robust Layout Elements

New constraint in physical design

“Forbidden elements”

EM-robust layout elements

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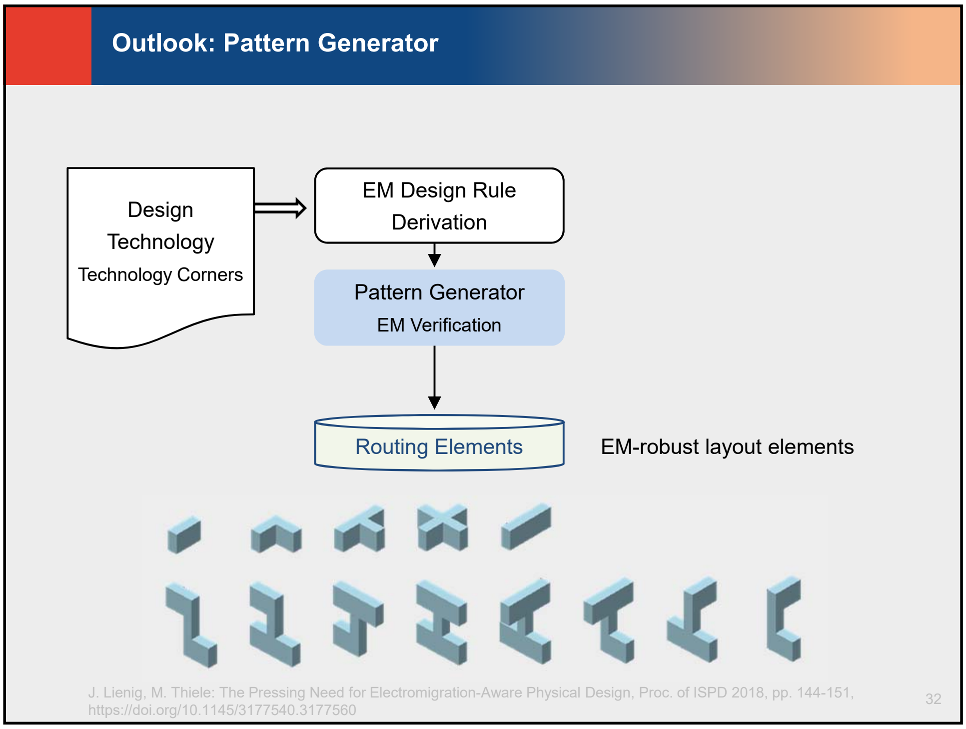

Outlook: Pattern Generator

Design
Technology
Technology Corners

EM Design Rule Derivation

Pattern Generator
EM Verification

Routing Elements

EM-robust layout elements

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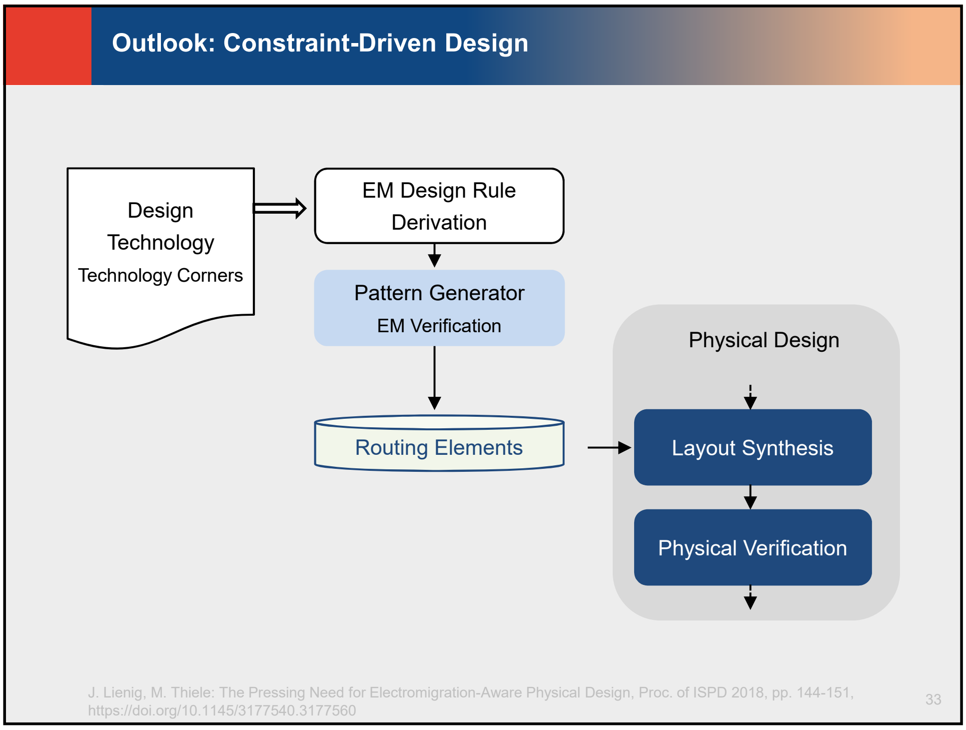

Outlook: Constraint-Driven Design

Design
Technology
Technology Corners

EM Design Rule Derivation

Pattern Generator
EM Verification

Routing Elements

Physical Design

Layout Synthesis

Physical Verification

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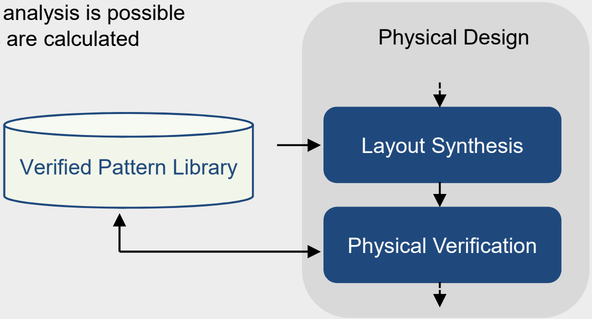
Outlook: Full-Chip Current Density Analysis

- Pattern library contains meta-models, that are mathematical relations between FE model constraints (boundary conditions) and result quantities, e.g. maximum current density
- Maximum current densities are calculated from the boundary conditions (currents) of the layout
- Full-chip current-density analysis is possible as only the meta models are calculated


Physical Design

Verified Pattern Library

Layout Synthesis

Physical Verification

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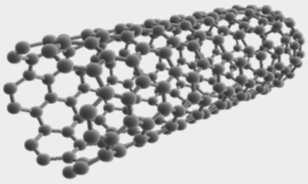
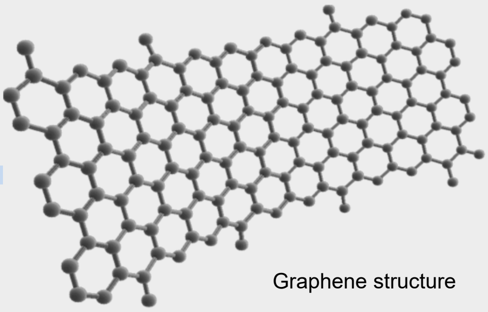
Outlook: New Materials


Carbon nanotube (CNT)


Graphene structure

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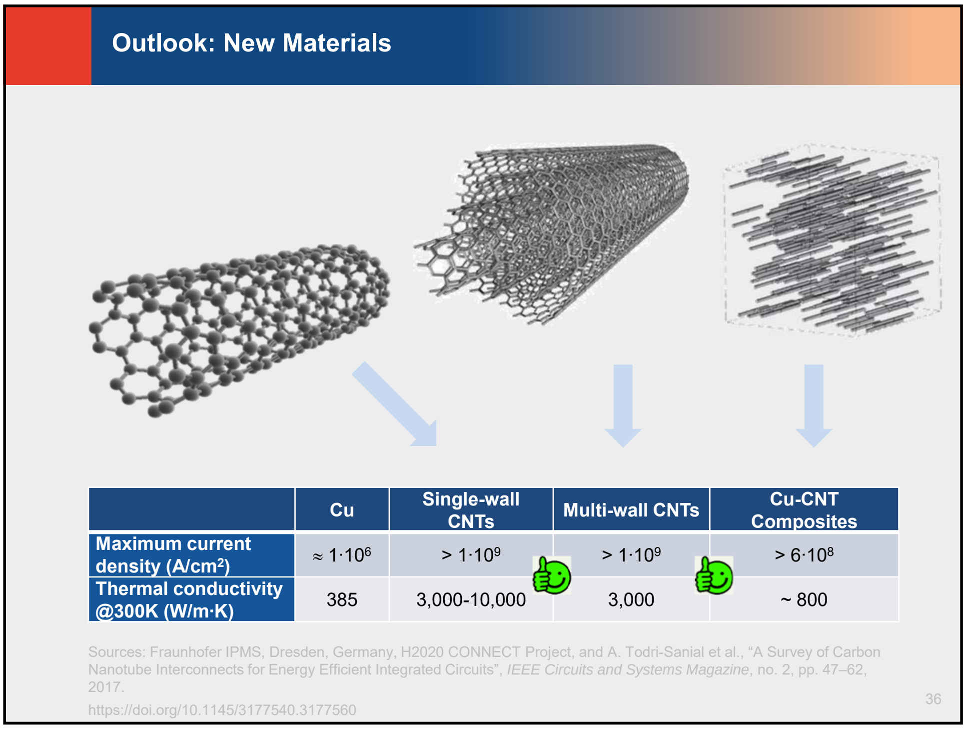
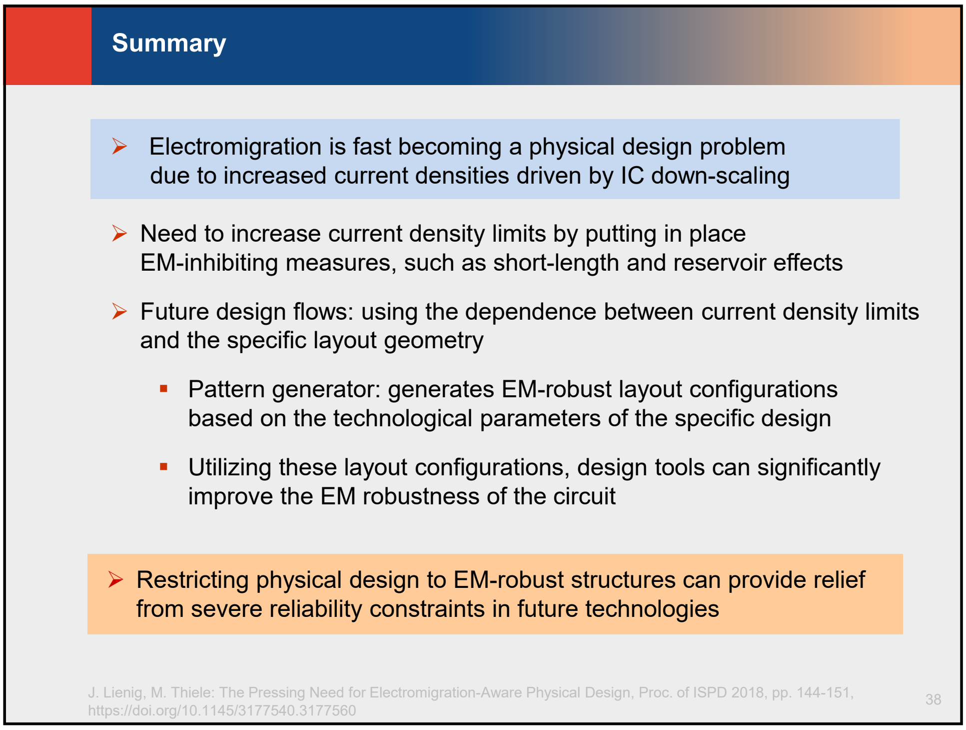


Outlook: New Materials

	Cu	Single-wall CNTs	Multi-wall CNTs	Cu-CNT Composites
Maximum current density (A/cm^2)	≈ $1 \cdot 10^6$	> $1 \cdot 10^9$ 👍	> $1 \cdot 10^9$ 👍	> $6 \cdot 10^8$
Thermal conductivity @300K (W/m·K)	385	3,000-10,000	3,000	~ 800

Sources: Fraunhofer IPMS, Dresden, Germany, H2020 CONNECT Project, and A. Todri-Sanial et al., “A Survey of Carbon Nanotube Interconnects for Energy Efficient Integrated Circuits”, *IEEE Circuits and Systems Magazine*, no. 2, pp. 47–62, 2017.

https://doi.org/10.1145/3177540.3177560



Summary

- ➢ Electromigration is fast becoming a physical design problem due to increased current densities driven by IC down-scaling
- ➢ Need to increase current density limits by putting in place EM-inhibiting measures, such as short-length and reservoir effects
- ➢ Future design flows: using the dependence between current density limits and the specific layout geometry
  - Pattern generator: generates EM-robust layout configurations based on the technological parameters of the specific design
  - Utilizing these layout configurations, design tools can significantly improve the EM robustness of the circuit
- ➢ Restricting physical design to EM-robust structures can provide relief from severe reliability constraints in future technologies

J. Lienig, M. Thiele: The Pressing Need for Electromigration-Aware Physical Design, Proc. of ISPD 2018, pp. 144-151, https://doi.org/10.1145/3177540.3177560

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