ROAD: Routability Analysis & Diagnosis Based on SAT Techniques

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UCSD VLSI LAB

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PHYSICAL DESIGN GETTING HARDER

- Keep Scaling Technologies
- Design Rule Complexity Rising

- Tons of design rules from multi-patterning technology
- Limited Resource (# of Routing Track)

Detailed Routing is getting complex and bottleneck.
I. Routability Analysis
**DESIGN RULE-CORRECT ROUTABILITY ANALYSIS**

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**Gate Netlist**

**Placement**

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**Given Pin-Layout**

**Power Rail**

**Routable?**

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**ILP: Optimal but 1048s (~18min) !**

**SAT: Not Optimized but 2s !!!!!**

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**SAT Method → Quick “go/no-go” Decision**
**Routability Analysis Framework**

- ILP-based routability optimization
- SAT-based routability analysis

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**Logic Simplification**
- ILP Patterns per ILP Formula
- Logic Minimizer Espresso [26]

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**Routability Analysis Flow**

1. **Testcase (i.e., Switchbox) Generation**
   - Inputs
     - #Vertical and Horizontal Tracks
     - Pin Density
   - Switchboxes
     - 3D Routing Graph
     - Source-Sink Definition

2. **SAT-Friendly ILP Formulation**

3. **ILP-to-SAT Conversion**

4. **Solvers**
   - ILP Solver CPLEX [27]
   - SAT Solver Portfolio
     - Plingling / Glucose-syrup / many-Glucose

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**Results of Routability Analysis**

- by ILP
- by SAT

- ILP Result: Routing Feasibility, Wirelength, Metal Cost, etc.
- SAT Result: Routing Feasibility, SAT Solution if Satisfiable

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PROPOSED ILP/SAT FORMULATION DIAGRAM

- The Multi-commodity network flow formulation (F)
- Conditional Design Rule (D)
- Layout Structure Map (L)

**Flow Formulation (F)**

- Commodity Flow Conservation (CFC)
- Exclusiveness Use of Vertex (EUV)

**Design-Rules Formulation (D)**

- 1. End-of-Line Space Rule (EOL)
- 2. Minimum Area Rule (MAR)
- 3. Via Rule (VR)

**Layout Structure Map (L)**

- Edge Assignment (EA)
- Metal Segment (MS)
- Geometry Variable (GV)
SAT FORMULATION – FLOW FORMULATION (F)

- **Commodity Flow Conservation (CFC)**
  - **CASE I)** Vertex ≠ source, sink: 0 or 2 edges uses
    1) Only one incoming/outgoing pair is allowable for all commodities.
    2) This commodity don’t use this vertex.

- **CASE II)** Vertex = source, sink: **Exactly-One (EO) Commodity Flow Constraint.**

\[
F_{CFC2}(v,n,m) = \text{EO}\left( \left\{ f^m_{m}(v,p) \mid p \in a(v) \right\} \right),
\]
\section*{SAT Formulation – Flow Formulation (F)}

- **Exclusiveness Use of Vertex (EUV)**
  - **CASE I.** Vertex ≠ source, sink: \textbf{At-Most-One (AMO) Net Constraint}
    
    1) Only one net can use a certain edge
    2) No Flow

    \[
    F_{EUV_1}(v) = AMO\left(\bigvee_{p \in a(v)} e_{v,p}^n \mid n \in N\right), \quad \forall v \in V
    \]

- **CASE II.** Vertex = source, sink: \textbf{Exactly-One (EO) Edge Constraint}

    \[
    F_{EUV_2}(v) = EO\left(\left\{ e_{v,p}^n \mid p \in a(v), n \in N \right\}\right), \quad \forall v \in V
    \]
**SAT FORMULATION – FLOW FORMULATION (F)**

- **Edge Assignment (EA)**

  \[ f_m^n(v,u) \rightarrow e_{v,u}^n \]

  \[ F_{EA}(e_{v,u}, n, m) = e_{v,u}^n \lor \neg f_m^n(v,u), \quad \forall e_{v,u} \in E, \forall n \in N, \forall t_m^n \in T^n \]

  Logical Imply. : edge is used by n net if m commodity of n net use this edge
  \( \rightarrow \) It requires for multi-commodity flow

- **Metal Segment (and Exclusiveness Use of Edge) (MS)**
  - Commander Encoding Variable of EO constraint of edge indicators

  \[ F_{MS}(e_{v,u}) = EO\left( \left\{ \neg m_{v,u} \right\} \cup \left\{ e_{v,u}^n \mid n \in N \right\} \right), \quad \forall e_{v,u} \in E \]
- **Geometric Variable (GV)**
  - End-of-Line indicator of each vertex for geometric conditional design rule.

\[
\begin{align*}
    g_{L,(1,v)} & = 1 \\
    g_{R,(2,v)} & = 1 \\
    g_{F,(v,1)} & = 1 \\
    g_{B,(v,2)} & = 1
\end{align*}
\]
SAT FORMULATION – DESIGN RULE FORMULATION (D)

- Minimum Area Rule (MAR)
  - A metal segment must cover at least three vertices (AMO Constraint)

\[
D_{MAR_LR}(\nu) = AMO(g_L,\nu, g_R,\nu, g_L,\nu_R, g_R,\nu_R), \\
\forall \nu \in V_2
\]

**Violation**

\[
\begin{align*}
g_R,\nu &= g_L,\nu_L = 1 \\
g_L,\nu &= g_R,\nu_R = 0
\end{align*}
\]

**No Violation**

\[
\begin{align*}
g_R,\nu &= 1 \\
g_L,\nu &= g_L,\nu_L = g_R,\nu_L = 0
\end{align*}
\]
**SAT FORMULATION – DESIGN RULE FORMULATION (D)**

- **End-of-Line (EOL) Space Rule**
  - The minimum distance between tips must be larger than 2 Manhattan distance (AMO Constraint)

\[
D_{EOL_R}(v) = \text{AMO}(g_R, v, g_L, v_{FR}) \land \text{AMO}(g_R, v, g_L, v_{BR}) \land \text{AMO}(g_R, v, g_L, v_{RR}),
\]

\[
\forall v \in V_2
\]

![Diagram showing various configurations with Violation and No Violation examples](image)
**SAT Formulation – Design Rule Formulation (D)**

- **Via Rule (VR)**
  - The distance between two vias should be larger $\sqrt{2}$ Euclidean Distance (AMO constraint)

$$D_{VR}(v) = \text{AMO}(m_{v, v_U}, m_{v_R, v_{UR}}, m_{v_B, v_{UB}}, m_{v_{BR}, v_{UBR}}) \land \text{AMO}(m_{v_D, v}, m_{v, v_U})$$

$\forall v \in V$
**Design Rule-Correct Routability Analysis**

- Flow Feasibility (F)
  - Conjunction of each subsets

\[
F = \bigwedge_{v \in V} \left( F_{EUV}(v) \land \bigwedge_{n \in N} \bigwedge_{t_m \in T^n} F_{CFC}(v, n, m) \right) \land \bigwedge_{e_{v,u} \in E} \left( F_{MS}(e_{v,u}) \land \bigwedge_{n \in N} \bigwedge_{t_m \in T^n} F_{EA}(e_{v,u}, n, m) \right)
\]

- Design Rule Formulation (D)

\[
D = D_{GV} \land D_{MAR} \land D_{EOL} \land \bigwedge_{v \in V} D_{VR}(v)
\]

- Design Rule-correct Routability (R)
  - L : Layout Structure Map → the geometry information of the switch box

\[
R = F \land D \land L
\]
II. Routability Diagnosis
NEXT STEP : ROUTABILITY DIAGNOSIS

- Conflict Diagnosis in Unroutable Case using SAT Technique
  - Exact Location of Conflict → Fast Trouble-shooting for Designer
  - Exact Conflict Relation → Guideline for Design Rule Manager

![Diagram of Power Rail with Unroutable Results]

- #V_Tacks = 9, #H_Tacks = 19
- PinDensity = 100%
- 21 Pins: 0-20
- 8 Outer Pins: 21-28
- 13 Nets: (9 13 17), (7 12 25), (0 6 28), (14 23), (16 19), (3 24), (2 22), (4 27), (8 18), (11 21), (15 20), (5 10), (1 26)
- Results: Unroutable
ROAD: OVERVIEW OF DIAGNOSIS

**Routability Analysis Using SAT Formulation**

*Unroutable Layout*

**MUS Extraction**
(Minimal Unsatisfiable Subset)

*Clause Minimization*

**Initial Propagation**
(Geometric Information of Switch-Box)

*Conflict Region*

**Decision (DLS)**
(Decision with Longest-Path Search)

**Propagation (PTA/PFA)**
(Propagation with True/False Assignment)

**Conflict Information**
(Conflict Geometry / Design Rule)

**Conflict?**

No

**DAG : H(U,D)**

**BCP Iteration**

**MUS**

**PIG**

Node : U (variable)

Edge : D (clause)

Unroutable Layout

*Conflict Region*

*Clause Minimization*

*Initial Propagation*

*Decision (DLS)*

*Propagation (PTA/PFA)*

**MUS Extraction**

**Conflict Information**
(1) **Minimal Unsatisfiable Subset (MUS)**

**Claim:** For every $\mathcal{F} \in \text{UNSAT}$, $\exists \mathcal{M} \subseteq \mathcal{F}$, such that $\mathcal{M} \in \text{MU}$.

**Pf:**
1. Let $\mathcal{M} = \mathcal{F}$.
2. If $\mathcal{M} \notin \text{MU}$, $\exists C \in \mathcal{M}$ such that $\mathcal{M} \setminus \{C\} \in \text{UNSAT}$.
3. Let $\mathcal{M} = \mathcal{M} \setminus \{C\}$, goto 2.

**Def:** $\mathcal{M}$ is *minimally unsatisfiable subformula (MUS)* of $\mathcal{F}$ if $\mathcal{M} \subseteq \mathcal{F}$ and $\mathcal{M} \in \text{MU}$.

**Notation:** $\text{MUS}(\mathcal{F})$ — the set of all MUSes of $\mathcal{F}$.

\[
\begin{align*}
C_1 &= (p) \\
C_2 &= (q) \\
C_3 &= (\neg p \lor \neg q) \\
C_4 &= (\neg p \lor r) \\
C_5 &= (p \lor q) \\
C_6 &= (\neg q \lor \neg r)
\end{align*}
\]

$\{C_1, C_2, C_3\}$ and $\{C_1, C_2, C_4, C_6\}$ are the (only) MUSes.
(2) **BCP (Boolean Constraint Propagation) & PIG**

- **PIG (Partial Implication Graph) in Our Framework**
  - Directed Acyclic Graph which Nodes are Variables, Edges are Clauses.
  - The implication relation between variable assignment from constraint clause

Clause set: \{ a \lor b , \neg a \lor c , \neg c \lor d , a \}

1st BCP, \( a = 1 \rightarrow \{c, \neg c \lor d\} \text{ remain} \)

2nd BCP, \( c = 1 \rightarrow \{d\} \text{ remain} \)

https://en.wikipedia.org/wiki/Unit_propagation
(3) **INITIAL PROPAGATION**

- Layout Structure Map (L) → Estimated Conflict Range

![Diagram with Power Rail and Estimated Conflict Region]

- **#V_Tracks** = 9
- **#H_Tracks** = 13
- PinDensity = 100%
- **14 Pins**: 0-13
- **8 Outer Pins**: 14-21
- **10 Nets**: {1 7 18}, {2 6 20}, {3 10}, {13 19}, {9 12}, {4 17}, {8 14}, {0 16}, {5, 15}, {11 21}

*Estimated Conflict Region*
(4) DLS (Decision with Longest-path Search)

- Longest-path search is most comprehensive explanation about failure
  - Via Position / Direction of Element are determined at DLS phase

- Conflict @ 2nd
- Conflict @ 1st
- Conflict @ 4th

Selected!
(5) PROPAGATION – PTA (WITH TRUE ASSIGNMENT)

- BCP propagation with True Assignment ($U_s$)

\[ v_U \rightarrow M_1 \]
\[ \text{VIA} (M_1 \rightarrow M_2) \]
\[ M_2 \]

$Pin_j$ (Supernode)
(5) PROPAGATION – PTA (WITH TRUE ASSIGNMENT)

▪ PTA Result of #1 VIA @ 9_13_100

- Blocked via (M₁ ↔ M₂)
- Blocked via (M₂ ↔ M₃)
- Assigned via (M₁ ↔ M₂)
(5) PROPAGATION – PFA (WITH FALSE ASSIGNMENT)

- BCP propagation with False Assignment ($U_s$)
  - Via-to-via spacing / Stacked – Via / Vias in same pin / element with direction against PTA

\[ v_{M_i} + v_{M_{i+1}} + v_{M_{i+2}} \]

\[ v_{FL} \quad v_F \quad v_{FR} \quad v_B \quad v_{BR} \quad v_{BB} \quad M_i \quad M_{i+1} \quad M_{i+2} \]

\[ v_{FL} \quad v_{UL} \quad v_U \quad v_{UR} \quad M_1 \quad M_2 \]

Blocked via

Blocked in-layer element
(5) PROPAGATION – PFA (WITH FALSE ASSIGNMENT)

- PFA Result of #1 VIA @ 9_13_100

- Blocked via (M₁ ↔ M₂)
- Blocked via (M₂ ↔ M₃)
- Assigned via (M₁ ↔ M₂)
- Blocked in-layer element

Diagram showing the propagation process with PFA (Partial Functional Assignment) and false assignment.
(6) DIAGNOSIS RESULT REPORT : EX) 9_13_100

- 4th via @ PFA phase → Conflict encounter!

□ Blocked via (M₁ ↔ M₂)

- Geometry : (Pin0) ↔ (7,10,1)
- Design Rule : CFC ↔ VR Rule

CONFLICT Information
- Geometry : (Pin0) ↔ (7,10,1)
- Design Rule : CFC ↔ VR Rule

\[ f_0^7(\text{pin0})(7,8,1) = 0 \]
\[ f_0^7(\text{pin0})(7,9,1) = 0 \]
\[ f_0^7(\text{pin0})(7,10,1) = 1 \]
\[ f_0^7(\text{pin0})(7,10,1) = 0 \]
III. ROAD Experimental Result
The Root causes of routing failure

- **Conflict Pin-shape (CP): Pin-Accessibility Problem!**
  - Simple-CP: Intrinsic Pattern in given Pin-layout
  - Propagated-CP: Simple-CP appears after some propagations

- **Routing Congestion**
  - The lack of routing resources such as #Track and #Layer

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**Table 2: Unroutable layout examples. \#N=\#Nets, \#P=\#Pins.**

<table>
<thead>
<tr>
<th>SwitchBox</th>
<th>Spec.</th>
<th>SAT Formulation</th>
<th>MUS</th>
<th>Conflict Cause</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>#N</td>
<td>#P</td>
<td>#Variable</td>
<td>#Clauses</td>
</tr>
<tr>
<td>11_7_80</td>
<td>6</td>
<td>12</td>
<td>16,776</td>
<td>378,551</td>
</tr>
<tr>
<td>9_19_100</td>
<td>13</td>
<td>29</td>
<td>101,943</td>
<td>5,368,125</td>
</tr>
<tr>
<td>9_13_100</td>
<td>10</td>
<td>22</td>
<td>54,884</td>
<td>2,280,223</td>
</tr>
<tr>
<td>12_13_70</td>
<td>10</td>
<td>23</td>
<td>79,471</td>
<td>3,478,371</td>
</tr>
<tr>
<td>11_7_90</td>
<td>7</td>
<td>14</td>
<td>21,014</td>
<td>580,925</td>
</tr>
<tr>
<td>7_7_100</td>
<td>4</td>
<td>9</td>
<td>7,972</td>
<td>110,389</td>
</tr>
<tr>
<td>7_13_100</td>
<td>7</td>
<td>15</td>
<td>24,236</td>
<td>595,898</td>
</tr>
<tr>
<td>15_7_90</td>
<td>9</td>
<td>20</td>
<td>45,782</td>
<td>1,725,676</td>
</tr>
<tr>
<td>19_13_70</td>
<td>15</td>
<td>33</td>
<td>171,092</td>
<td>11,287,222</td>
</tr>
</tbody>
</table>

- Simple-CP
- Propagated-CP
- Routing Congestion
UNROUTABLE LAYOUT CLASSIFICATION – SIMPLE-CP

- Simple-CP with 3-3-n-3-3 pattern

Simple Intrinsic CP Pattern

3 – 3 – n – 3 – 3
**UNROUTABLE LAYOUT CLASSIFICATION – PROPAGATED-CP**

- **Propagated-CP**: Main Concern of Pin-accessibility
  → Why designer don’t change Pin-shape?

**Propagated CP Pattern**

- #V_Tracks= 12, #H_Tracks= 13
- PinDensity= 70%
- 14 Pins: 0-13
- 9 Outer Pins: 14-22
- 10 Nets: {2 13 14}, {10 12 15}, {4 8 21}, {0 22}, {6 20}, {3 16}, {7 17}, {5 11}, {9 19}, {1 18}
Routing Congestion: Technology Limitation Identification!

- #V_Tracks= 15, #H_Tracks= 7, PinDensity= 90%
- 12 Pins: 0-11
- 8 Outer Pins: 12-19
- 9 Nets: \{2 11 14\}, \{5 8 13\}, \{3 15\}, \{6 12\}, \{9 16\}, \{1 4\}, \{7 19\}, \{0 17\}, \{10 18\}

All tracks are occupied / blocked!!
Routability Diagnosis Experimental Statistics

- Total Diagnosis Time
  - MUS Extraction Time + Decision & Propagation Time
  - Diagnosis Performance (Complexity and Execution Time) depends on the root causes of routing failure
    - CP pattern case is less than 30 seconds on average to get the result.
    - Routing Congestion Case is relatively longer than the CP pattern cases.

Table 3: Experiment statistics of routability diagnosis (94 pin layouts @ 90 grids). In the table, #N=#Nets, #P=#Pins.

<table>
<thead>
<tr>
<th>Conflict Type</th>
<th>#N (avg.)</th>
<th>#P (avg.)</th>
<th>#Variable (avg.)</th>
<th>#Clauses (avg.)</th>
<th>Diagnosis Time [s] (avg.)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Original</td>
<td>MUS</td>
</tr>
<tr>
<td>CP pattern (80 cases)</td>
<td>10.2</td>
<td>22.4</td>
<td>68,954.6</td>
<td>3,068,017.3</td>
<td>291.5</td>
</tr>
<tr>
<td>Routing Congestion (14 cases)</td>
<td>10.0</td>
<td>22.5</td>
<td>68,803.3</td>
<td>3,049,687.6</td>
<td>2,627.8</td>
</tr>
</tbody>
</table>
The same Grid Number with different number of pins row

- (a) 20_7_80
  - Simple-CP: 31%
  - X (unknown): 0%
  - Total: 69%

- (b) 11_13_80
  - Simple-CP: 80%
  - Propagated-CP: 12%
  - Routing Congestion: 8%

- (c) 8_19_80
  - Simple-CP: 80%
  - Propagated-CP: 20%
  - Routing Congestion: 0%
1. Ilgweon Kang, Dongwon Park, Changho Han, Chung-Kuan Cheng. “Fast and Precise Routability Analysis with Conditional Design Rules”. SLIP 2018
3. Journal Extension is now under preparation. (TCAD)
Appendix
### TABLE I

**NOTATIONS FOR SAT FORMULATION.**

<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>( G(V,E) )</td>
<td>Three-dimensional (3-D) routing graph</td>
</tr>
<tr>
<td>( V )</td>
<td>Set of vertices in the routing graph ( G )</td>
</tr>
<tr>
<td>( V_d )</td>
<td>Set of vertices in ( d )-th metal layer of the routing graph ( G )</td>
</tr>
<tr>
<td>( v )</td>
<td>A vertex at the coordinate ( (x_v,y_v,z_v) )</td>
</tr>
<tr>
<td>( \nu_d )</td>
<td>0-1 indicator if ( d )-directional adjacent vertex about ( v )</td>
</tr>
<tr>
<td>( a(v) )</td>
<td>Set of adjacent vertices of ( v )</td>
</tr>
<tr>
<td>( E )</td>
<td>Set of edges in the routing graph ( G )</td>
</tr>
<tr>
<td>( e_{vu} )</td>
<td>An edge between ( v ) and ( u, u \in a(v) )</td>
</tr>
<tr>
<td>( N )</td>
<td>Set of multi-pin nets in the given routing box</td>
</tr>
<tr>
<td>( n )</td>
<td>( n )-th multi-pin net</td>
</tr>
<tr>
<td>( s_n )</td>
<td>A source of ( n )</td>
</tr>
<tr>
<td>( t_n )</td>
<td>Set of sinks in ( n )</td>
</tr>
<tr>
<td>( t_m )</td>
<td>( m )-th sink of ( n )</td>
</tr>
<tr>
<td>( f_m )</td>
<td>( m )-th commodity flow of ( n ) heading to ( t_m )</td>
</tr>
<tr>
<td>( e_{vu,m} )</td>
<td>0-1 indicator if ( e_{vu,m} ) is used for ( n )</td>
</tr>
<tr>
<td>( f_m(v) )</td>
<td>Flow variable on ( v ) for commodity ( f_m )</td>
</tr>
<tr>
<td>( e_{vu,m} )</td>
<td>0-1 indicator if ( e_{vu,m} ) is used for commodity ( f_m )</td>
</tr>
<tr>
<td>( m_{vu} )</td>
<td>0-1 indicator if there is a metal segment on ( e_{vu} )</td>
</tr>
<tr>
<td>( g_{d,v} )</td>
<td>0-1 indicator if ( v ) forms ( d )-side EOL of a metal segment</td>
</tr>
</tbody>
</table>

**PIN #1**  ✠✠✠✠✠  **Power Rail**  ✠✠✠✠✠  **H-Track**

| **V-Track**  ✠✠✠✠✠  **Grid**  ✠✠✠✠✠  **Outer-Pin Connection** | **PIN #1**  ✠✠✠✠✠  **Power Rail**  ✠✠✠✠✠  **H-Track** |

![Diagram of M₁ in G](image1)

![Diagram of M₂ in G](image2)

![Diagram of M₃ in G](image3)

![Diagram of M₄ in G](image4)
**What is SAT (Boolean Satisfiability)?**

- **SAT** (Boolean Satisfiability)
  - Find a variable assignment to make propositional logic formula evaluates to 1 (True) (Satisfiable), or prove that no such assignment exists (Unsatisfiable)

\[
A \cap (\neg B \cup C) \quad \rightarrow \quad A \rightarrow 1, B \rightarrow 1, C \rightarrow 1 \quad \text{(Satisfiable)}
\]

\[
A \cap B \cap (\neg B \cup \neg A) \quad \rightarrow \quad \text{Unsatisfiable}
\]

- Usually, Product of Sum (i.e. CNF) is normal representation for SAT formula

<table>
<thead>
<tr>
<th>X</th>
<th>Y</th>
<th>F(x,y)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**Truth Table**

**Product of Sum (CNF)**

\[
(\neg X \cup Y) \cap (X \cup \neg Y)
\]

**Sum of Product (DNF)**

\[
(X \cap Y) \cup (\neg X \cap \neg Y)
\]

**Clause**

**Equivalent Representations**