Via Pillar-aware Detailed Placement

Yong Zhong, Tao-Chun Yu, Kai-Chuan Yang, and Shao-Yun Fang

The Electronic Design Automation Laboratory
Department of Electrical Engineering
National Taiwan University of Science and Technology
INTRODUCTION
Detailed Placement

- In the VLSI physical design flow, placement consists of 3 stages:
  1. Global placement
  2. Legalization
  3. Detailed placement

- Detailed placement focuses on improving the legalized placement solution, while keeping its legality.
Feature size has shrunk down to 7 nm and beyond

- The impact of wire resistance is significantly growing
- The circuit delay incurred by the metal wires is noticeable raising

A new technique “Via Pillar” (or via pillar) is proposed

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L. -C. Lu, Physical Design Challenges and Innovations to Meet Power, Speed, and Area Scaling Trend", ISPD, 2017
Structure of Via Pillar

- Multiple vias
- Multiple metal wires
- Cross multiple layers (generally)
Benefits of Via Pillar

- Reduce Wire Resistance
- Reduce Circuit Latency
- Enhance Reliability
- Enhance EM robustness
Benefits of Via Pillar

L. -C. Lu, Physical Design Challenges and Innovations to Meet Power, Speed, and Area Scaling Trend", ISPD, 2017
Problem on Via Pillar Insertion

Major issues that cause poor Insertion success rate:

- Track Alignment Issue
- Power/Ground Stripe Overlapping
- Insufficient Margin Area
Track Alignment Issue

- In our experiments, we found that the via pillar insertion may fail when the access point is not at a certain position w.r.t. its adjacent tracks.

M4 (success)  M4 (failure)
In our experiments, we found that the via pillar insertion may fail when the access point is not at a certain position w.r.t. its adjacent tracks.
If the structure overlaps with a power/ground (PG) stripe, the insertion of the via pillar will fail.

Denser or wider PG strips will result in fewer eligible positions, more difficult to optimize the result.
If a via pillar structure overlaps with another via pillar or design boundaries, the insertion will fail.
Previous Works

The research on detailed placement have been developed in decade that address various issues

- Wirelength
- Density
- Manufacturing rules
- Lithography
- Multi-row-height Cells

However, none of these works has focused on via pillar insertion in the detailed placement stage
Terminology

- **An N-cell** is a cell that is not concerning via pillar (normal cell).
- **A V-cell** is a cell that will be inserted a via pillar.
- **An eligible row/site/position** indicates the position with maximized insertion rate:
  - No track alignment issue
  - No overlap with any PG stripe
- **MDC** is the maximum displacement constraint that prevents from a large movement.
Algorithm Flow

- Input
- Eligible Positions Determination
- Global Move
- Legalization for V-cells
- Legalization for N-cells
- Check Legality
  - Yes
  - No
- Global Move for Congested Row Improvement
- Output
Input

- Placement Result
- Configure file

List of via-pillar inserting cells
To enhance the via pillar insertability, we determine all the eligible positions for all V-cells.

1. Filter out positions overlap with PG stripe
2. Filter out positions with track alignment issue
The goal of this step is to move all V-cells in ineligible rows to eligible sites.

Find a best eligible position for a source V-cell.

The best eligible position is...?

- An N-cell
  - Swap
- A V-cell or a white space
  - Move
Global Move (cont’d)

- For each V-cell, we first find a best eligible position.
- We traverse all eligible sites within $MDC$ and evaluate them by the cost function:

$$cost = \alpha \cdot \Delta W + \beta \cdot D + \rho P_C + \sigma (1 - P_S)$$

$$P_C = \frac{Area(Ncells)}{Area(Row)} \cdot \Delta Area(cell)$$

$$P_S = \frac{\#eligible\ sites}{\#total\ sites\ in\ row}$$

$\Delta W$: Wirelength improvement (or degradation)

$D$: Displacement

$P_C$: Penalty of congested situation

$P_S$: Penalty of density of eligible sites
Global Move (cont’d)

- The overlaps among cells are permitted in this step
- To prevent from the sequence issue, we move a cell to a site if it is occupied by another V-cell

Find a best eligible position for a source V-cell

The best eligible position is… ?

- An N-cell
- A V-cell or a white space

- Swap
- Move

- There should be no V-cell in an ineligible row after this step
Our legalizer is based on dynamic programming-based detailed placement algorithm [Taghavi et al., ICCAD, 2010]
However, the order of cells among V-cells and N-cells may have to be changed to obtain a result in better quality if the PG stripes are dense or the row is congested.
Hence, we divide legalization procedure into two-stage to achieve the effect of re-ordering.

Legalization for **V-cells**
- Resolve overlaps among **V-cells**
- Ignore the existence of **N-cells**

Legalization for **N-cells**
- Regard the **V-cells** as obstacles
- Achieve the effect of re-ordering among **V-cells** and **N-cells**
In the legalization of V-cells, we ignore the existence of N-cells and only legalize for V-cells.
Legalization for V-cell (cont’d)

\[
\text{cost} = \alpha \cdot \Delta W + \beta \cdot D + P_M + P_E
\]

\(\Delta W:\) Wirelength improvement (or degradation)

\(D:\) Displacement

\(P_M:\) Penalty for violation of MDC

\(P_E:\) Penalty of eligible site alignment

\[
P_M = \begin{cases} 
0, & \text{displacement within MDC} \\
\infty, & \text{displacement beyond MDC}
\end{cases}
\]

\[
P_E = \begin{cases} 
0, & \text{if the site is eligible,} \\
\infty, & \text{otherwise.}
\end{cases}
\]
Legalization for N-cell

- To achieve the effect of re-ordering among V-cells and N-cells, we regard the V-cells as obstacles without actually placing it.
Legalization for N-cell (cont’d)

Cell

Movement (-M~M)
Legalization for N-cell (cont’d)

Cell

\[ C_i \quad \rightarrow \quad C_{i+1} \quad \rightarrow \quad C_{i+2} \quad \cdots \quad \rightarrow \quad C_{i+n} \]

Movement (-M~M)

S \rightarrow -M+2 \rightarrow \cdots \rightarrow M \rightarrow \cdots \rightarrow T

\[ M \rightarrow -M+1 \rightarrow -M+2 \rightarrow \cdots \rightarrow M \rightarrow \cdots \rightarrow M \]
Legalization for N-cell (cont’d)

\[ \text{cost} = \alpha \cdot \Delta W + \beta \cdot D + P_M \]

\(\Delta W:\) Wirelength improvement (or degradation)
\(D:\) Displacement
\(P_M:\) Penalty of MDC

\[ P_M = \begin{cases} 0, & \text{displacement within MDC} \\ \infty, & \text{displacement beyond MDC} \end{cases} \]
Global Move For Congested Row Improvement

- After legalization, some of the rows are still remaining illegal when cells are highly congested in the rows.
- We try to move the cells in a congested row to white spaces with a smallest cost within $MDC$.

Diagram:

1. Find a target white space with lowest cost
2. Move
3. Legalization
Global Move For Congested Row Improvement

\[
\text{cost} = \alpha \cdot \Delta W + \beta \cdot D + \epsilon P_V
\]

\(\Delta W\): Wirelength improvement (or degradation)

\(D\): Displacement

\(P_V\): Penalty of local overlap

\[P_V = \text{overlap area with adjacent cells}\]
EXPERIMENTAL RESULTS
Environment Setting

- C++ programming language
- The results were generated on a 2.10 GHz Intel Xeon CPU E5-2620 Linux machine with 32GB memories
- Parallel processing in the eligible position determination by 24 threads
- Adopt commercial APR tool “IC Compiler 2” to perform via pillar insertion process
Benchmarks

- We integrate the real industrial 16 nm standard cell library into ISPD 2015 placement contest
- Only big-macro-free testcases were adopted
- We create a via-pillar structure which crosses from M1 to M5, with 1, 2, 2, 2 bars and 1, 1, 2, 2 cuts in M2, M3, M4, M5, respectively
- We manually lay PG stripes in each testcase

<table>
<thead>
<tr>
<th>Design</th>
<th>Cell Area ($mm^2$)</th>
<th>#Cells</th>
<th>#Nets</th>
</tr>
</thead>
<tbody>
<tr>
<td>mgc_fft_1</td>
<td>0.0584</td>
<td>32281</td>
<td>33037</td>
</tr>
<tr>
<td>mgc_fft_2</td>
<td>0.0584</td>
<td>32281</td>
<td>33037</td>
</tr>
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<td>mgc_des_perf_1</td>
<td>0.1790</td>
<td>112644</td>
<td>112878</td>
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<tr>
<td>mgc_matrix_mult_1</td>
<td>0.2427</td>
<td>155825</td>
<td>158527</td>
</tr>
</tbody>
</table>

Characteristics of Benchmark Suit
## Result on Testcases with PG Stripe

- With PG Stripe & track alignment issue

<table>
<thead>
<tr>
<th></th>
<th>fft_1</th>
<th>fft_2</th>
<th>des_perf_1</th>
<th>matrix_mult_1</th>
<th>Average</th>
</tr>
</thead>
<tbody>
<tr>
<td>#Row</td>
<td>192</td>
<td>192</td>
<td>348</td>
<td>383</td>
<td></td>
</tr>
<tr>
<td>#Eligible row</td>
<td>96</td>
<td>96</td>
<td>174</td>
<td>192</td>
<td></td>
</tr>
<tr>
<td>#Cell</td>
<td>32281</td>
<td>32281</td>
<td>112644</td>
<td>155325</td>
<td></td>
</tr>
<tr>
<td>#V-cell</td>
<td>3850</td>
<td>3832</td>
<td>955</td>
<td>13103</td>
<td></td>
</tr>
<tr>
<td>Insertion rate % (bef.)</td>
<td>41.26</td>
<td>44.28</td>
<td>40.31</td>
<td>42.56</td>
<td>42.1025</td>
</tr>
<tr>
<td>Insertion rate % (aft.)</td>
<td>99.13</td>
<td>99.25</td>
<td>99.01</td>
<td>99.16</td>
<td>99.1375</td>
</tr>
<tr>
<td>ΔInsertion rate %</td>
<td>57.87</td>
<td>54.97</td>
<td>58.7</td>
<td>56.6</td>
<td>57.035</td>
</tr>
<tr>
<td>HPWL(before)</td>
<td>5.73E+08</td>
<td>5.63E+08</td>
<td>2.84E+09</td>
<td>2.93E+09</td>
<td></td>
</tr>
<tr>
<td>HPWL(after)</td>
<td>5.92E+08</td>
<td>5.80E+08</td>
<td>2.84E+09</td>
<td>2.98E+09</td>
<td></td>
</tr>
<tr>
<td>ΔHPWL</td>
<td>+3.37%</td>
<td>+2.91%</td>
<td>+0.01%</td>
<td>+1.88%</td>
<td>+2.04%</td>
</tr>
<tr>
<td>Displacement</td>
<td>3.33E+07</td>
<td>3.18E+07</td>
<td>5.25E+07</td>
<td>1.10E+08</td>
<td></td>
</tr>
<tr>
<td>Total movement of Vcell</td>
<td>1.19E+07</td>
<td>1.11E+07</td>
<td>6.24E+06</td>
<td>3.21E+07</td>
<td></td>
</tr>
<tr>
<td>Average mov. (Row Hei.)</td>
<td>1.82</td>
<td>1.70</td>
<td>3.91</td>
<td>1.46</td>
<td>2.22253</td>
</tr>
</tbody>
</table>

- With PG Stripe & track alignment issue
Layout of Testcases with PG Stripe

- $mgc_{fft\_1}$
- $matrix\ mult\ 1$
Furthermore, we evaluate our algorithm on the testcases without impact from PG stripes

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<td></td>
</tr>
<tr>
<td>Insertion rate % (bef.)</td>
<td>48.02 %</td>
<td>51.35 %</td>
<td>47.23 %</td>
<td>49.41 %</td>
<td>49.0025 %</td>
</tr>
<tr>
<td>Insertion rate % (aft.)</td>
<td>99.57 %</td>
<td>99.34 %</td>
<td>99.89 %</td>
<td>99.31 %</td>
<td>99.5275 %</td>
</tr>
<tr>
<td>ΔInsertion rate %</td>
<td>51.55 %</td>
<td>47.99 %</td>
<td>52.66 %</td>
<td>49.9 %</td>
<td>50.525 %</td>
</tr>
<tr>
<td>HPWL (before)</td>
<td>5.73E+08</td>
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<td>5.91E+08</td>
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<td>2.82E+09</td>
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<td></td>
</tr>
<tr>
<td>ΔHPWL</td>
<td>+3.30%</td>
<td>+2.98%</td>
<td>-0.69%</td>
<td>+1.32%</td>
<td>+1.73%</td>
</tr>
<tr>
<td>Displacement</td>
<td>4.30E+07</td>
<td>4.19E+07</td>
<td>9.85E+07</td>
<td>1.58E+08</td>
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We evaluate our algorithm on the testcases without impact from track alignment issue

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<td></td>
</tr>
<tr>
<td>Insertion rate % (bef.)</td>
<td>85.74</td>
<td>85.87</td>
<td>85.45</td>
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<td>85.5775</td>
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<tr>
<td>Insertion rate % (aft.)</td>
<td>99.05</td>
<td>99.12</td>
<td>99.26</td>
<td>99.24</td>
<td>99.1675</td>
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<tr>
<td>ΔInsertion rate %</td>
<td>13.31</td>
<td>13.25</td>
<td>13.81</td>
<td>13.99</td>
<td>13.59</td>
</tr>
<tr>
<td>HPWL(before)</td>
<td>5.73E+08</td>
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<td>2.88E+09</td>
<td></td>
</tr>
<tr>
<td>ΔHPWL</td>
<td>-0.79%</td>
<td>-0.97%</td>
<td>-0.64%</td>
<td>-1.56%</td>
<td>-1.00%</td>
</tr>
<tr>
<td>Displacement</td>
<td>2.39E+07</td>
<td>2.37E+07</td>
<td>8.64E+07</td>
<td>1.01E+08</td>
<td></td>
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<tr>
<td>Average mov. (Row Hei.)</td>
<td>0.63</td>
<td>0.65</td>
<td>3.52</td>
<td>0.50</td>
<td>1.32</td>
</tr>
</tbody>
</table>
CONCLUSION
Conclusion

- We propose first placement framework considering via pillar insertibility maximization in detailed placement stage.
- We explore the possible causes of insertion failure and also verified these reasons through experiments.
- The experimental results show that through this algorithm, even if the solution space has been reduced by PG stripes and track alignment issue, we can still achieve a solution with high insertion rate.
THANKS FOR LISTENING