On Pioneering Nanometer-Era Routing Problems

An Appreciation
of Professor CL Liu’s visionary approach to Physical Design

Tong Gao and Prashant Saxena
Synopsys, Inc.

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Introduction

• A true anecdote…
  – At an early 90s conference, a presenter told the story of searching under a lamppost
    – Joke about theoretician stereotypes
  – Prof. Liu stood up to defend theoreticians
• Motto: search for interesting problems and solutions, pique interest and fellowship
• Numerous contributions by Prof. Liu
  – Transforming EDA from ad hoc heuristics to algorithmic research
    – Pioneered works in logic synthesis, floorplanning, placement, routing, …
  – Predicting future EDA challenges, and stimulating innovative research
    – Illustrated in this presentation with examples in modern routing area
Importance of Predicting the Future

- Complex EDA problems take years to converge
  - Industry moves to a new node quickly
  - Solutions are needed shortly after difficulties first encountered
    - Example: mad scramble for 20nm DPT
  - Fill the gap between academia and industry
    - Industry is pre-occupied with tactical revenue driven issues
    - Academia and research institutes are best suited to research into future difficult problems

The Free Dictionary
Challenges and Rewards of Researching into the Future

• Challenges
  – Requires strong vision and intuition to predict the future
    – Takes instinct, and years of experience and observation
    – With Prof. Liu, it is a consistent trait
      – For example, his real time scheduling work
  – Requires strong leadership and drive to initiate research into new areas
  – Requires keen sense of judgment along the way and flexibility to adjust
    – Flexibility to adjust: my first topic (optical switch routing) dropped in half a year
    – Continued focus when on the right track: years of research into Channel Routing

• Rewards
  – Accredited as pioneers of new areas
  – Exert leadership and gain fellowships
  – Easier to publish papers – great news for students😊
    – Not the easy way out though – others need to agree with the topics’ relevance
  – …
Prof. Liu’s Early Works in Routing

• Early works focused on Channel routing problems
  – Influential early work done by Prof. Kuh’s group
    – “Efficient algorithms for channel routing”, TCAD’82, T Yoshimura and ES Kuh
  – Prof. Liu’s group was one of the most active research groups in early 80s
    – “A new channel routing problem”, DAC’83, HW Leong and CL Liu
    – “Permutation channel routing”, ICCD’85, HW Leong and CL Liu
    – “Simulated annealing channel routing”, ICCAD’85, HW Leong, DF Wong, and CL Liu
    – “Compact channel routing with via placement restriction”, VLSI’86, DF Wong and CL Liu
    – …
  – Extended to multi-layer channel and over the cell routing
    – “A new approach to three- or four-layer channel routing”, TCAD’88, J Cong, DF Wong, and CL Liu
    – “Over the cell channel routing”, ICCAD’88, J Cong and CL Liu
    – …
  – Extended to FPGA architecture
    – “A channel router for single layer customization technology”, ICCAD’91, Y Sun, SK Dong, S Sato, and CL Liu
    – “Two channel routing algorithms for quickly customized logic”, EDAC’93, SK Dong, Y Sun, S Sato, and CL Liu
    – …
Routing Problems in 80s and early 90s

• Router’s role: maximize route completion with minimal wirelength
  – Little attention to performance
    – Delay dominated by cells – little attention to wire RC
    – Homogenous metal stacks with few routing layers – little need for timing-driven layer assignment
  – Feature sizes much larger than litho wave length
    – Few, simple design rules
  – Most routing related research was in topology generation

• Routing was mostly an industry chip-finishing step
  – Relatively few research activities
Routing Technology Industry Trend

*Timing aspect*

- Semi industry: new process node every 2 years
  - Devices become faster, while interconnect wires become thinner with closer proximity
    - Circuit performance: more dominated by interconnect Rs and Cs
    - Significant crosstalk impact on circuit performance
  - Layer stacks become very heterogeneous
    - RC varies as much as 50x between layers,
    - Significant timing variation due to layer assignment
- Design sizes explode with emphasis on low power
  - Wires travel over longer distances
  - Weaker drivers
- *Interconnect optimization is becoming the center-stage of physical design*

Bohr, “Intel's 65 nm Logic Technology”, Aug. 2004
Routing Technology Industry Trend

Process aspect

- Semi industry: new process node every two years
  - Litho technology cannot keep up with shrinking feature sizes
    - Major jump in complicated design rules
    - Need for other innovations such as redundant via insertion and double/triple patterning (DPT/TPT)
Predicting the Future

• Vision is always 20/20 in retrospective
  – Difficult to see today’s routing trends in 80s & 90s
  – It would be too late to start on today’s problems now

• Crucial to start EDA research before a process is ready

• Prof. Liu’s crystal ball…
  – Asked me to work on crosstalk driven routing in 1992
    – “Minimum crosstalk channel routing”, T Gao and CL Liu, 1993
  – Today
    – Over the next decade, spurred much academic research with many publications
    – One of the most emphasized areas in timing optimization in industry today
Crosstalk Driven Detailed Routing

• Crosstalk driven routing: an unique marriage between an important future problem with an algorithmic approach
  – Channel routing is a track assignment problem with vertical constraints
  – Crosstalk can be roughly modeled with parallel wires on adjacent tracks
  – Mixed integer linear programming solver advanced significantly in 90s
  – Crosstalk driven channel/switchbox routing problems was formulated as mixed integer linear programming problem
    – Optimize track/layer permutation to optimize for crosstalk and wire length

• Impact on EDA industry
  – The exact formulation is not used now as industry moved to area routing
  – Set an algorithmic direction to solve crosstalk problem during routing
  – Brought great awareness of crosstalk and spurred much research
    – Many papers published.
  – Laid foundation to today’s crosstalk driven routing solutions
    – Industry routers today still control wire spacing and layers for crosstalk control
Predicting the Future (cont.)

• Prof. Liu’s crystal ball...
  – Advised Prashant to work on timing-driven layer assignment in 1997
  – Today
    – Layer stacks can be very heterogeneous, with many routing layers and RC variations among layers as much as 50x
      – Layer assignment can dominate wire delay
    – Timing-driven layer assignment is crucial to design closure

Bohr, “Intel's 65 nm Logic Technology”, Aug. 2004
Performance Driven Layer Assignment

• The challenge was to balance routability against net criticality during layer assignment
  – Addressed timing-driven layer assignment in the context of congestion-related tradeoffs inside a router
  – Introduced a dynamically adjusted “quota” for each net to ameliorate net ordering problem
    – Prevents early-routed nets from monopolizing the “good” layers
  – Used congestion-aware “lookahead key” to evaluate delay impact of moving to next layer

• Impact on EDA industry
  – The notion of “historical congestion” of a gcell implicit in dynamic quotas is the basis of “negotiated” routing in modern routers
  – Layer assignment has increasing effects on timing convergence in increasing number of designs
    – Router needs to be layer RC aware
    – Physical synthesis needs to model the layer assignment
Routing Technology Industry Trend

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The DNA Lives On

Continuing Prof. Liu’s Tradition…

• Antenna effect
  – Seminal work on routing with diode insertion

• Redundant Via Insertion
The DNA Lives On
Continuing Prof. Liu’s Tradition...

• OPC routing
  – P. Yu and D. Z. Pan, "TIP-OPC: A New topological invariant paradigm for pixel based optical proximity correction”. ICCAD, 2007
  – P. Yu and D. Z. Pan, "A Novel Intensity Based OPC Algorithm with Speedup in Lithography Simulation”. ICCAD, 2007

• CMP routing
The DNA Lives On
Continuing Prof. Liu’s Tradition…

• Double patterning
  – K. Yuan and D. Z. Pan, "WISDOM: Wire Spreading Enhanced Decomposition of Masks in Double Patterning Lithography", ICCAD, 2010

• Triple patterning
The DNA Lives On
Continuing Prof. Liu’s Tradition…

• E-beam
  – K. Yuan and D. Z. Pan, “E-beam lithography stencil planning and optimization with overlapped characters”, *ISPD, 2011* (Best Paper Award)
  – S.-Y. Fang and Y.-W. Chang, "Graph-based subfield scheduling for electron-beam photomask fabrication," *ISPD, 2012*

• EUV
Current and Upcoming Challenges

• Process challenges – mismatch between feature sizes and litho technology continues
  – Growing complex design rules hurt run time and QoR
    – Is there a more scalable approach?
      – Design-rule compilers?
      – Restrictive patterns?
    – What is next after LELE DPT and possible solutions?

• Timing challenges – interconnect delay impact needs to be modeled and optimized throughout physical synthesis
  – Pre-route optimization
    – How to better model routing interconnect?
    – How to ensure correlation without over-constraining routing?
  – Post-route optimization
    – Needs stronger better integrated ECO flow between routing and optimization

• …
Thank You Prof. Liu!!!

• For help in transforming EDA from ad hoc heuristics to algorithmic research
• For foreseeing future challenges, and pioneering and leading researches into them
• For being the best advisor possible