

# **Maximum Current Estimation Considering Power Gating**

**Fei Li and Lei He**

**ECE Dept.**

**University of Wisconsin – Madison**

**<http://eda.ece.wisc.edu>**

# Significance of Maximum Current

- **Maximum Current Affects Power/Ground wires**
  - Electromigration
  - IR voltage drop
  - Ground bounce
  - $Ldi/dt$  inductive noise
- **Excessive Maximum Current may cause**
  - Permanent circuit failure
  - Logic malfunction
  - Timing error

# Maximum Current Estimation

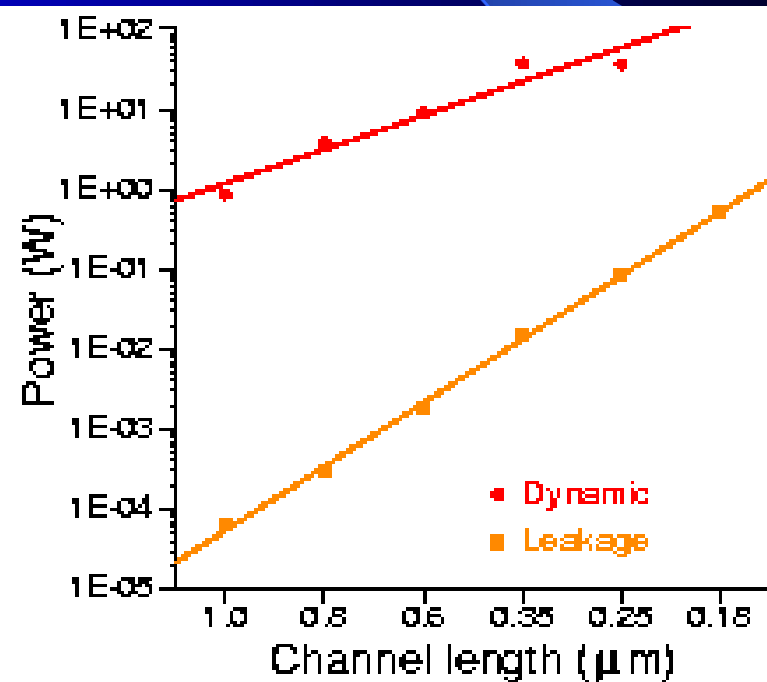
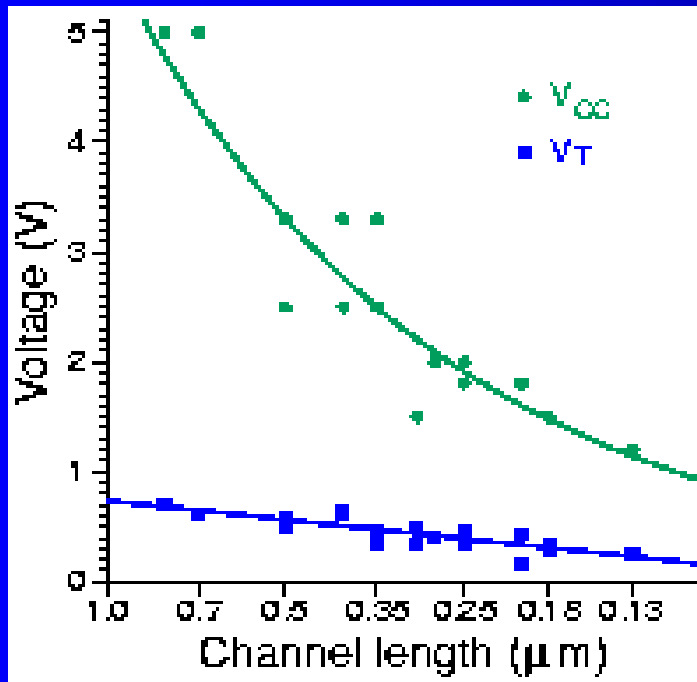
- **Previous Work**
  - Find two input vectors that cause maximum switching current
- **Various Approaches Proposed**
  - Simulation-based
  - ATPG-based

# DSM Scaling

- **The Scaling Trend in Semiconductor Industry**
  - Scaling down of supply voltage ( $V_{dd}$ )
  - Reduction of transistor threshold voltage to compensate for performance loss
- **Dynamic Power**
  - Offset by the scaling down of  $V_{dd}$
- **Leakage Power**
  - Increases exponentially when threshold voltage scales down
  - Anticipated to be comparable to dynamic power in a few generation

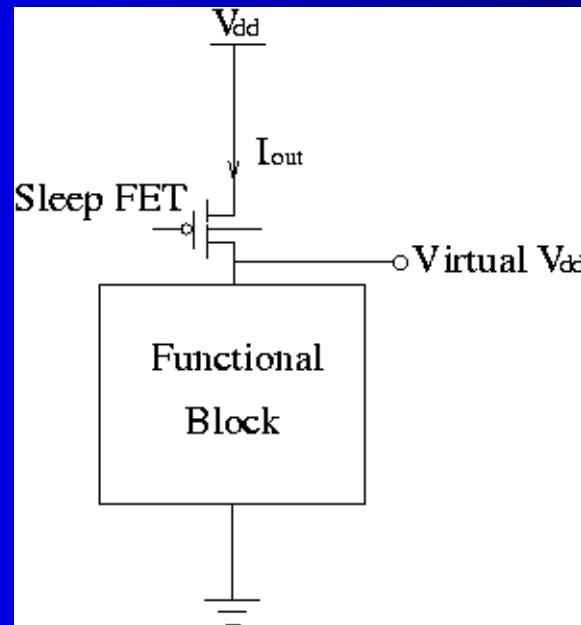
# Power Trend

- Intel's microprocessor in the past few technology generations
- Leakage power soon becomes comparable to dynamic power

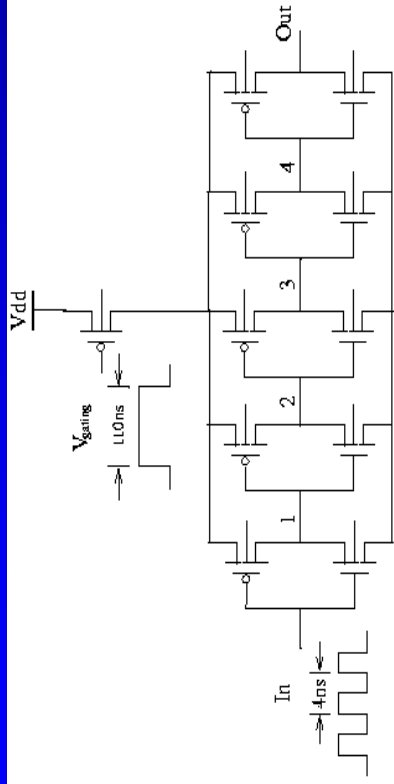


# Power Gating

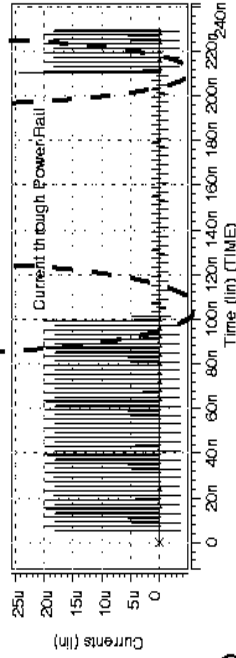
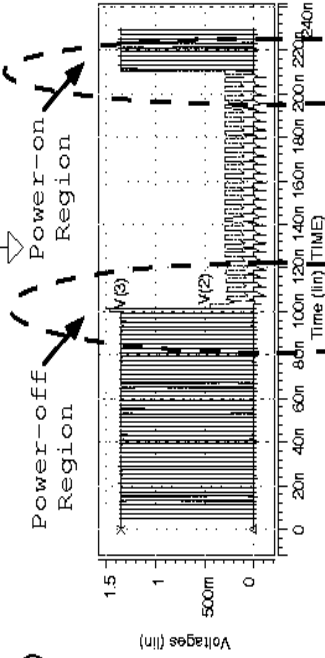
- Sleep transistor to power on or power off the circuit
- Power gating reduces leakage power as well as dynamic power



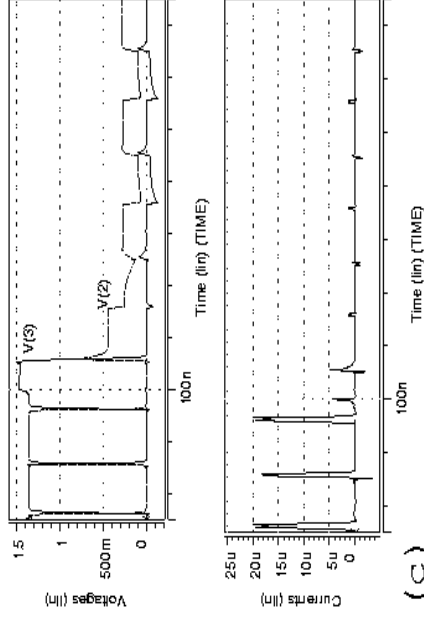
# Impact of Power Gating



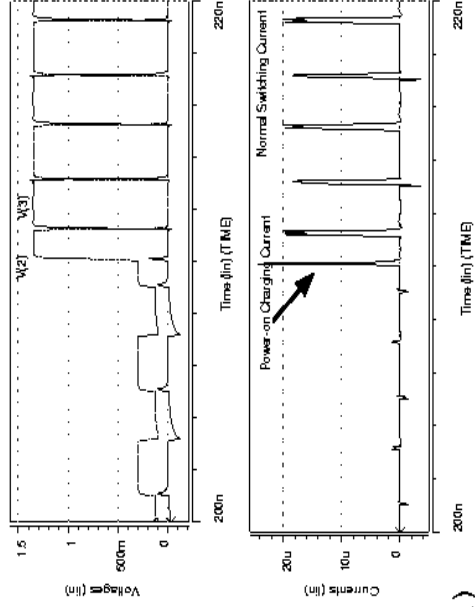
(a)



(b)



(c)



(d)

# Issues of Power Gating

- **Phenomena:**
  - All the gate output nodes in the functional unit will be discharged quickly during sleep mode
  - Significant current spike is observed when the functional unit is powered on again
- **Power-on current is different from normal switching current**
  - Dependent on one vector as the initial state is always “0”
  - Related to size of sleep transistor and P/G noise

# Algorithm

- **Assumption**
  - The power-on charging current is proportional to the total charge to be restored after wake-up
- **Objective**
  - Maximize the total stored charge after the functional unit is powered on
- **Two Algorithms proposed by using ATPG technique**
  - Fanout-based Algorithm  *$I_{max}/Fanout$*
  - Gain-based Algorithm  *$I_{max}/Gain$*
  - Both are heuristic algorithms

# Fanout-based Algorithm

## *Imax/Fanout*

- **Figure of merit for the maximum current**

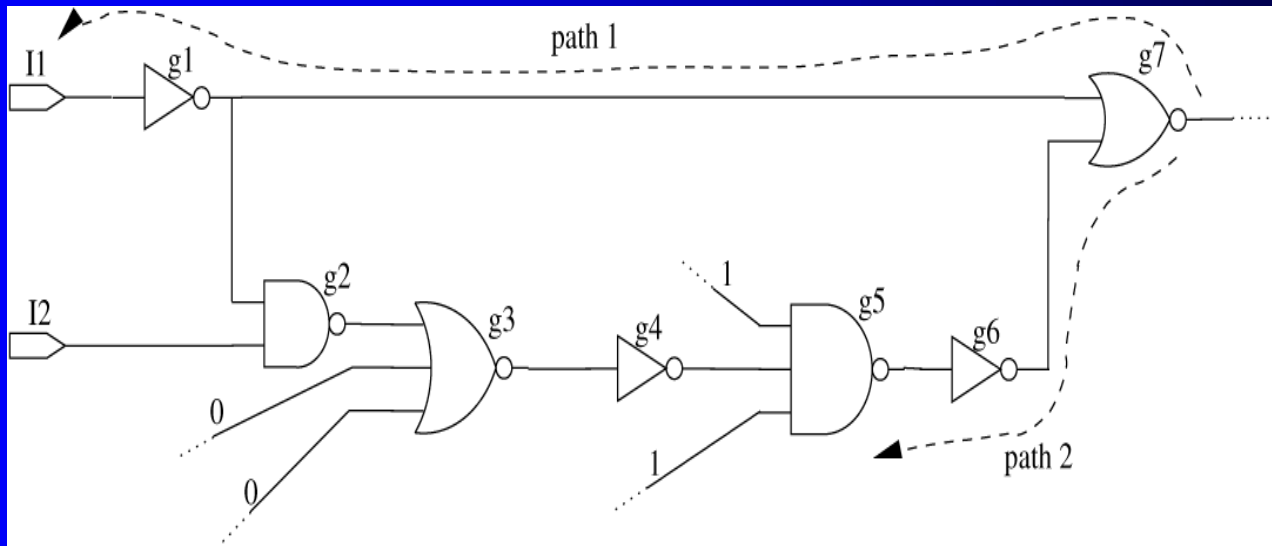
$$P_i = \sum_{\text{for all the gates}} VAL(g) \cdot F_{out}(g) \cdot V_{dd}$$

- $VAL(g)$  is the logic value of gate  $g$ ,  $F_{out}(g)$  is the load capacitance of gate  $g$ .
- **It is a greedy algorithm**
  - **Assign logic value 1 to gates in a greedy fashion**
  - **Fanout determines the order of gates to be assigned**

# Fanout-based Algorithm

## *Imax/Fanout (cont)*

- Test generation technique is used to resolve the conflicts and get the input vector
  - Backtracing to choose the path that may maximize the assignment of value 1
  - Backtracking to resolve the conflicts



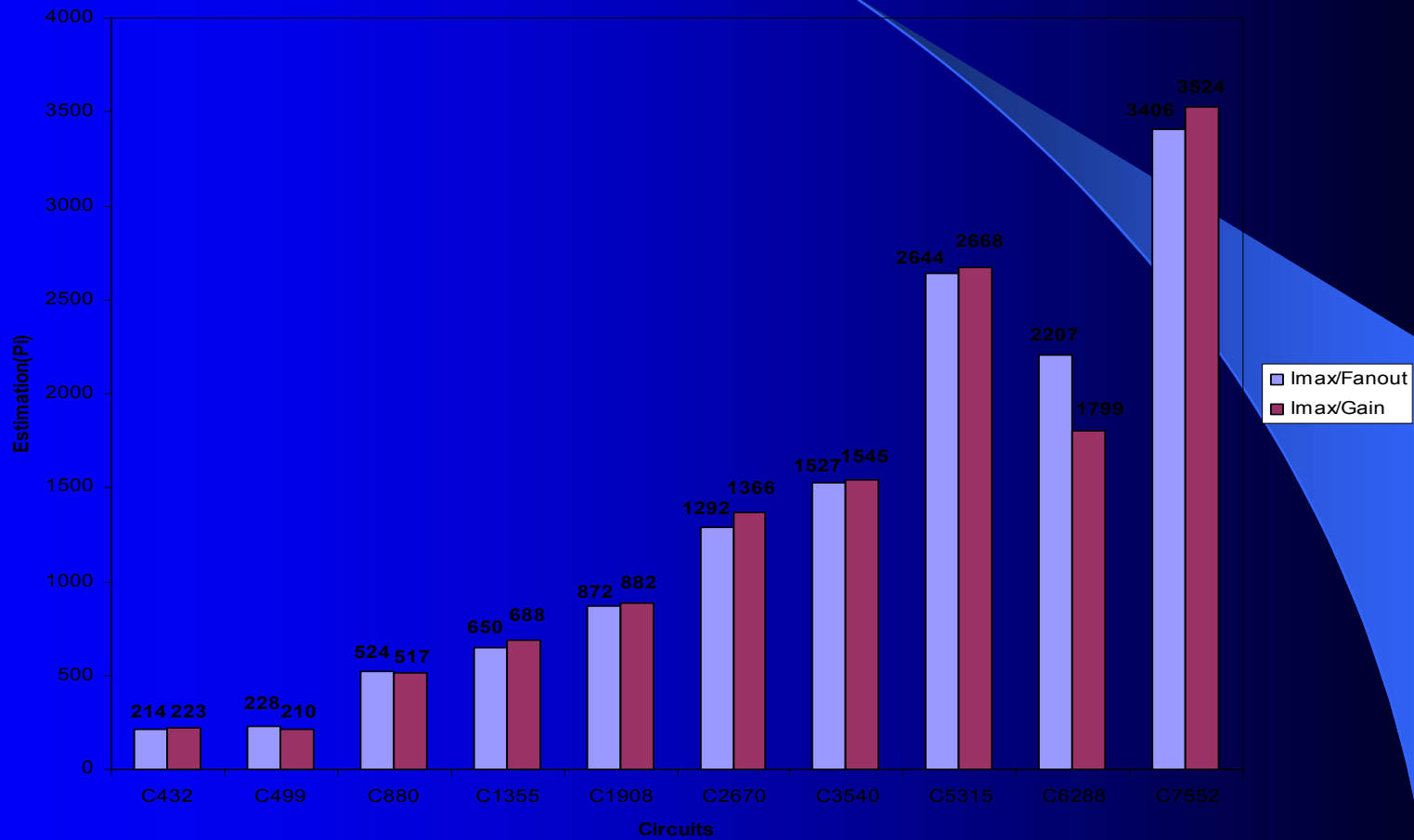
# Gain-based Algorithm *Imax/Gain*

- The fanout-based metric is somewhat local
- *Gain* defined as the new metric for each gate output to observe more globally
- Gain is computed by *implication* of the assignment

$$gain(g, v) = (-1)^{(v+1)} \cdot F_{out}(g) + \sum_{h \in IMP} ((-1)^{V(h)+1} \cdot F_{out}(h))$$

- Both *g* and *h* stand for gates
- *IMP* is the set of gates whose outputs are implied by the assignment
- Gain is the global effect of one assignment within its implication range

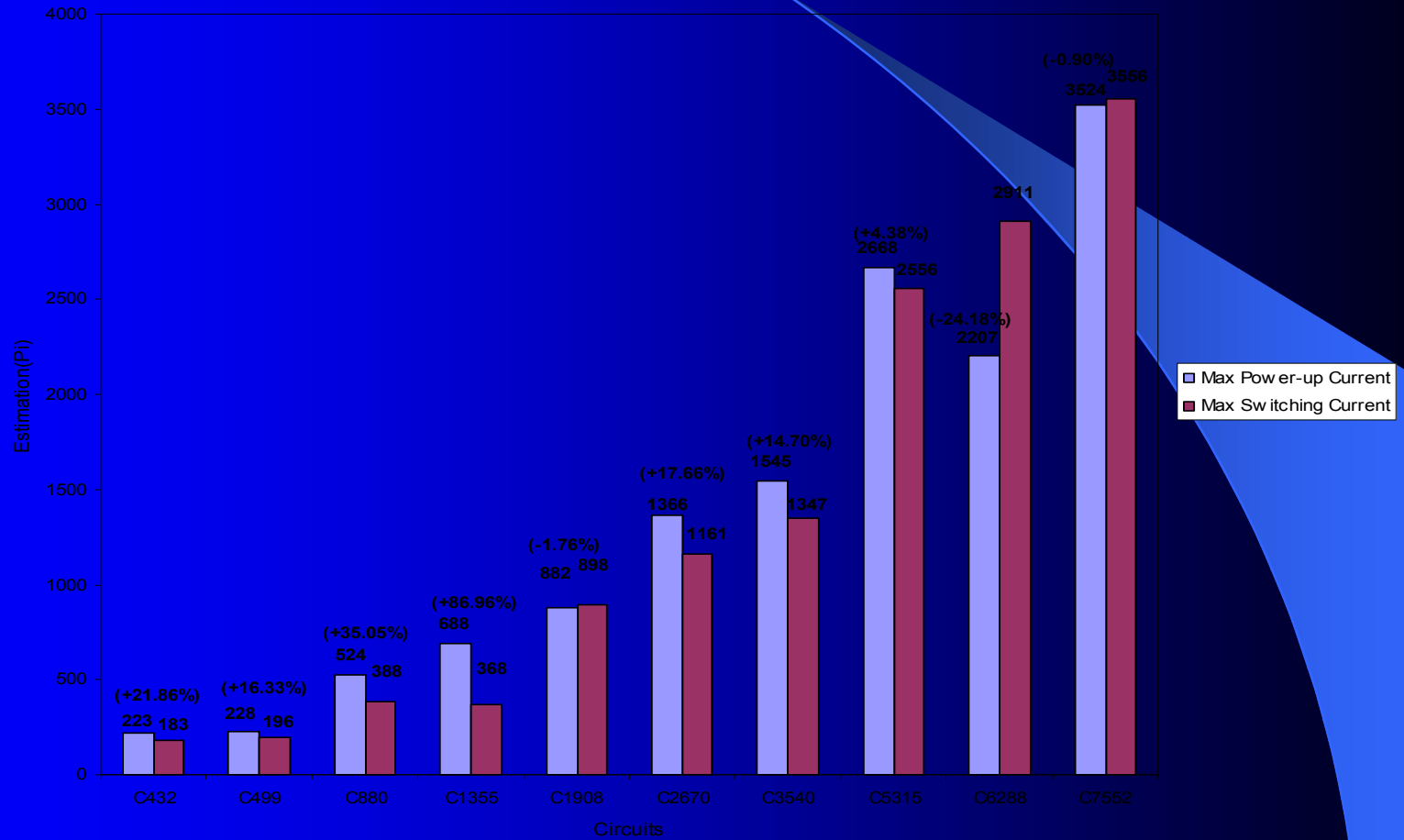
# Imax/Fanout vs Imax/Gain



# Runtime

Circuit	Runtime(sec)	
	<i>I</i> <sub>max</sub> / <i>F</i> <sub>anout</sub>	<i>I</i> <sub>max</sub> / <i>G</i> <sub>ain</sub>
C432	0.08	0.12
C499	0.15	0.24
C880	0.22	0.3
C1355	0.37	0.93
C1908	0.53	1.48
C2670	2.02	1.87
C3540	1.63	6.23
C5315	4.72	4.48
C6288	3.48	6.13
C7552	9.25	9.63

# Switch Current vs Power-on Current



# Conclusion

- **Power Gating may lead to more severe reliability problem**
- **Maximum Current Estimation Considering Power Gating should be used to guide P/G wires planning and optimization**