Industrial Clock Synthesis

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Outline

• Problems that our customers care about
• Existing solutions and plan-of-record solutions
• Improvements required
Clock Network

• Clock network delivers the clock signal to synchronize every sequential cell in the clock domain
Clock Network Metrics

• Power

• Insertion delay for a clock path
  - Usually longer than the clock period
  - Proxy for variation and power
  - Logic level
  - RC delay

• Skew under variation
  - False skew
  - Variation
    - Multiple corners
    - OCV (on-chip variation)
Power: Clock → Major Culprit

• Power: biggest implementation issue today
  - Consumer electronics
  - Frequency limiter: 4GHz ceiling

• Biggest trouble maker
  - Clock
    - 1/3 total power
    - Many large and leaky buffers
Variation: Clock → Most Susceptible

• Variation: biggest implementation issue tomorrow
  ▪ Frequency limiter
    • >40% dead cycle time
  ▪ Consumer electronics
• Biggest trouble maker
  ▪ Clock
    • OCV impact: 2X
Variation: Clock $\rightarrow$ Most Susceptible

- MC CTS: how to minimize skew for all corners?
  - Variation ratios of cells and wires differ in different corners
    - Variation ratios of wires differ in different layers
    - Failed chips $\leftrightarrow$ hold violation caused by variable skews
  - Skew = 5-5 = 0; Skew = 5.7-5.6 = 0.1
Performance

• Performance: biggest implementation challenge yesterday?
  - 1G Hz ASICs

• Clock skew is still a big issue for performance today
  - More clocks, more modes and more IPs
  - Complex clock gating
  - Higher wire delays
Clock Is Key

- Not competitive in clock $\rightarrow$ not competitive in timing or power for 45nm and beyond
- State-of-the-art clock-tree synthesis algorithms
Industrial Solutions for Power

• Clock gating
  ▪ Conventional
  ▪ Sequential
  ▪ Physical clock gating
• Register clumping
• Register banking
Clock Gating Used by 90% of Synopsys Users

- Clock Gating: 90%
- Gate-Level Power Optimization: 51%
- Multi-Voltage Design: 43%
- Multi-Threshold Design: 42%
- StateRetention/MTCMOS: 18%
- Power Network Synthesis: 14%

Please check the techniques your team is using on your current project.
2007 N = 718; Margin of error = +/- 4%
Clock Gating

- Automatic clock gating
  - `always@(posedge clk)
    if (en) Q <= D`
- ICGs (Integrated Clock Gating cells)
  - Fewer sizes and uneven loads $\rightarrow$ harder to balance skew
  - Consume power
Physical Clock Gating

• Design Compiler inserts ICGs during logic synthesis
  ▪ ICG drive flops wide-spread for datapath timing; unbalanced ICG levels
  ▪ Leave power saving opportunities on the table
ICG Merge

- Merge ICGs of the same enable signal
ICG Removal

• Remove ICGs that are ineffective (small fanout and mostly enabled) or causing unbalanced ICG levels
ICG Splitting

• Split ICGs based on timing, DRC and placement
Issue: Higher ICGs

- Merging ICGs with the same enable may save more clock tree power
  - Can gate a larger subtree
- Splitting ICGs make enable signal timing more easily satisfied
Issue: Higher ICGs

- Does not always save power!
  - Higher ICGs restrict the sharing of the subtrees
  - May introduce enable timing violations
Issue: Multi-Layer ICGs

- Multi-layer ICGs may save more clock tree power
  - DC PwrC generates multi-layer ICGs by enable factoring
  - May gate a larger subtree

![Diagram of multi-layer ICGs with factor and removal steps]
Issue: Multi-Layer ICGs

- But does not always save power!
  - Multi-layer ICGs restrict sharing of the subtrees
  - Extra ICG may consume more power than a very small gated subtree
Flop Placement: Register Clumping

- Around 8% reduction in total power on average
Flop Placement: Register Banking

- Automatically place registers into banks
  - Reduce power
  - Reduce clock skew
  - Implemented as RP (relative placement) constraints
  - *Routability may be an issue for some designs*
Industrial Solutions for Variation

- Clock meshes
- OCV-aware clustering
Clock Meshes

• Good skew under variation
  ▪ Tree above the mesh
  ▪ Trees below the mesh to drive the flops

• Bad for power
  (~+30% clock power)
  ▪ More wires
  ▪ Can only gate the small clock trees below the mesh

• Few SNPS customers mass-produce IC products with clock meshes

• Insight from clock mesh?
  ▪ Regularity → good for variation
Dummy ICG Insertion

• Insert dummy ICGs to balance topology
OCV-Aware Register Clustering

- Try to cluster registers with critical timing paths in between within a 1st or 2nd level cluster → minimize variation impact to timing
Register Clumping

- Place registers closer for the leaf-level buffers or ICGs to minimize leaf-level net capacitance (>50% of total net cap)
Register Banking

• Place registers into rectangular banks (more dramatic form of register clumping)
Regular Clock Tree Synthesis

- Synthesize regular buffer tree based on DRC and placement
  - Balanced buffer levels, ICG levels, fanout, wire length (by placement), metal layer
Industrial Solutions for Timing

- Clock routing
- Useful skews
- Inter-clock delay balancing
- CTS for SoCs
- Multi-voltage-domain and multi-mode CTS
Clock Routing

- Signal routing mostly for routability (wire length) and timing
- Clock routing mostly for skew under variation and power (wire length)
- Snaking for skew under variation
- Selective shielding clock nets to control skew
Detail-Route Clocks with Wire Snaking

- Detail route the clock tree using minimal wire snaking (and shielding) to fine-tune skew

![Diagram of clock tree routing](image)
Before Physical Synthesis

- Irregular gated clock topology bad for variation and power
After Physical Synthesis

- Regular gated clock topology good for variation and power
Useful Skew

• Clock skews can be used to fix timing violations
  ▪ Setup: trigger the launcher sooner and/or the capturer later
  ▪ Hold: trigger the launcher later and/or the capturer sooner

• Risk
  ▪ Clock skew is hard to control under variation
Inter-Clock Delay Balancing

• If there are timing paths from one clock domain to another clock
  • Inter-clock delay must be balanced based on the timing constraints
    • Extra insertion delay is bad for power and variation
CTS for SoCs

• SoC
  ▪ Large number of IPs with known clock latencies
    • Hard to balance skews
  ▪ Large number of placement and/or routing blockages
    • Hard to balance topology
  ▪ Multiple voltage domains and multiple operation modes
    • Multiple clocks
    • Complex requirements
Multiple Voltage Domains and Multiple Modes

- Clock shared by multiple voltage domains
  - No timing path in between → insert isolation cells near the top of the clock tree to save power
- Clock going through a voltage domain that may be turned off in an operation mode
  - Clock buffers powered by always-on power rail
    - Implication in power rail synthesis
Summary

• Competitive clock synthesis technology is key for IC product differentiation
  ▪ Power
  ▪ Variation
  ▪ Performance

• Academic research in this area will make huge impacts to the real world through the realization of cool, robust and fast ICs
Backup Slides
Pipelined Datapath with Bubbles

- Invalid data (bubbles) may go through the pipelined datapath and consume energy during computation
Conventional Clock Gating

- Gate clock upon invalid data
  - always @(posedge clk)
    if (vld) begin a1 <= a0; b1 <= b0; end
Sequential Clock Gating

- Introduce a valid-bit pipeline to track valid data and gate the clock to the datapath so that no pipeline stage computes for invalid data.