Impact of Manufacturing on Routing Methodology at 32/22 nm

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Outline

- ASIC detail router challenges at 32/22nm
  - Library density and design size
  - Complexity of DRC rules
  - DFM consideration
  - Double Pattern (DP) methodology

- Methodology Impact
  - Accuracy
  - Pre-calculation
  - Prevention
Density

- High density libraries at 32nm
  - M2 PG rails
  - M1 M2 pins
  - Dense library cells cause routing problems

- Aggressive rules
  - Modeling vias and short connections in Global Route

- Size of designs exceeds > 10M instances
  - Geographic database
  - NlogN is not enough
Density: M2 Library

- M2 PG rails and M2 pins:
  - Reduced routing resources
  - Limits possibility for pin connection
  - M3 stripe can cause a trap

M1 pins are in a “trap” formed by M2 rails and M3 stripe

M1 pin surrounded by M1/M2 shapes

M2 rail

M2 rail

M3 stripe
Density: Aggressive Rules

- Global router requires precise modeling
  - Via is not a point anymore
  - Need to consider min area and EOL rules
  - Small connections in gcell affects M2/M3 resources
Density: Size of Designs

- Design size is a challenge
  - 30M design → 1 Billion of wires and vias
  - Geographic database after 1M
- N*log(N) can be expensive for N – need n*log(n)

```c++
LargeData {}; vector<LargeData> data; sort(data);
{ ... swap(N1, N2); ...}
```

```c++
LargeData {}; vector<LargeData*> data; sort(data);
{ ... swap(n1*, n2*); ...}
```
DRC Complexity

- DRC rule count
  - Increase in number of rules
  - Increase in number of ranges per rule

- Complexity
  - Actual polygon processing
  - Multiple objects result in a violation
  - Pessimistic and simple models do not work anymore

- Various approaches
  - Post processing of layout
  - Integration of DRC engine with router
DRC: Number of Rules and Complexity

- Manufacture uses 193nm light to print 32nm feature

What you see is not what you get
# DRC: Number of Rules and Complexity

- Increase in DRC rules to address printability issues

<table>
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<tr>
<th>Rule</th>
<th>130nm</th>
<th>90nm</th>
<th>65nm</th>
<th>45nm</th>
<th>32nm</th>
<th>22nm</th>
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<td>Width-based spacing</td>
<td>1-2</td>
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<td>3-4</td>
<td>4-5</td>
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<td>1.5 pitch</td>
<td>2 pitch</td>
<td>2.5 pitch</td>
<td>3 pitch</td>
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<td>Min-Step (OPC)</td>
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<tr>
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<tr>
<td>Fat Jog (OPC)</td>
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DRC: Complexity of Verification

- Complex polygon operations
  - build polygon for shape
  - perform 5 reshape operations
  - check via enclosure vs. resulted blue contour

- Multiple objects in a violation
  - two wires (green) with W1 and S1 between two other wire corners (CA CB)
  - if no any objects in BoxB1 BoxB2 then OPC will create bridge violation
DRC: Complexity for Router

- Complex shape-dependent rules is a challenge
  - How to consider the track?
    - Pessimistic – loose via
    - Optimistic – bad long wire
  - Spacing = FUN(width, parallel length)

- “Shadowing” grid points do not work
  - There are many “gray” areas around shapes where router should be accurate
  - Router should understand length dependent rules
  - Router should dynamically change solution from “history”
DRC: Complexity for Router

- Addressing complex violations
  - Post processing fixing
    - Easy to implement
    - Not guaranteed
- Integration with DRC engine
  - Difficult to implement
  - Best approach

DRC engine annotates candidates for rerouting

Search & Repair

Notch fill results in new fat shape which now violates spacing
DRC: Router Integration

- Requirement for DRC/DFM closure at 32m/22nm
  - Decouple verification from core router
  - Use polygon based DRC engine
  - Integrate core router with various signoff tools

Diagram:
- Router Search&Repair
- Router verification
- Polygon DRC verification
- Signoff DRC verification
- Litho/ hot spot detection
DFM Requirements

- DRC clean does not mean good yield
  - Any angle is the problem for manufacturing
  - Any via is object for failure

- Preferred routing style
  - Enclose via in pin – library pre-calculation
  - Minimize fat shapes – wire/via relations
  - Minimize non-preferred direction

- Various DFM approaches
  - Post processing
  - Concurrent routing with reservation of room
  - Pins pre-calculation for DFM vias
DFM: Preferred Routing Style

- Via inside of pin, short M1 connections
- Minimize fat shapes and jogs on top layers

ideal routing picture
DFM: DFM Via Approaches

- Pre-calculate library for DFM

- Concurrent DFM via usage in routing
  - Many vias leads to excessive runtime
  - Aggressive via insertion leads to unrecoverable violations
  - Space reservation
Double Patterning at 20nm – Another Magnitude Increase in Complexity

- New dimension for routing tasks
  - Multiple schemes of DP
  - Non-formalized rules because DP is a synthesis process
  - Coloring is the core for DP process
  - Global conflict vs. local marker

- Various manufacturing solutions
  - Conservative to flexible

- Routing solutions
  - DRC prevention rules
  - Integration with signoff tools
  - Own coloring algorithm
**DP: Problem Statement**

- Create two or more masks
  - Metal line stays as CD
  - Spacing is increased to 3xCD
DP: Problem Statement

Different DP Methodologies

- SIT (SADP): Sidewall Image Transfer (Self Align DP)
- LELE: litho-etch, litho-etch
- Can be mixed in the process
- Every Fab have their own methodology
DP: Manufacturing Dilemma

- DP methodology is still evolving
  - No experience on design side for DP conflict resolution
  - Unknown manufacturing cost and design impact
  - No agreement on the best approach

Process constraints

- unidirectional fixed pitch
- correct by construction minimal impact
- unrestricted
- fully embedded DP detection and fixing

solution is here?
area trade off

Design flow
DP: Global Conflict in Routing

- DP problem is not localized as regular DRCs
  - Reroute can result in violation on another portion of the chip
  - Incremental approach is broken

S&R window: router does not see objects outside

Initial DRC violation

Object is rerouted to fix DRC

New conflict due coloring
**DP: Global Conflict in Routing**

- Conflict contour can include too many objects
  - DP detection does not tell who is the reason of violation
  - Several objects can be the reason in a big contour
DP: Routing Approach

- Prevention by DRC rules
  - Restrictions for non-preferred direction
  - Spacing depending on direction
  - Track routing only

- DP verification
  - Own coloring engine
  - Integration with signoff

- Repair of DP conflicts is still an open question
Modern Detail Router architecture

- Pin density analysis, Pin access for DFM vias pre-calculation
- Via and small connections modeling in Global router
- DRC polygon verification
- Signoff DRC verification
- Litho detection
- DP detection
- Support for length dependent rules
- Preferred Routing Style
- Concurrent DFM optimization
- DP prevention
Summary

- 32/22nm technology complexity stressing traditional models, methodologies and algorithms
  - Advanced DRC
  - DFM
  - DP

- A new routing architecture is needed for predictable and efficient manufacturing closure
  - Adaptable to evolving methodologies vis-à-vis cost vs. benefit
  - Concurrent verification and design
  - Signoff driven prevention and repair