

**ISPD 2015**  
**Blockage-Aware**  
**Detailed Routing-Driven**  
**Placement Contest**  
**Benchmark Design Suite**

---

**[www.ispd.cc/contests/15/ispd2015contest.html](http://www.ispd.cc/contests/15/ispd2015contest.html)**

**March 3, 2015**

# Outline

1. Motivation
2. Benchmark Suite
3. Placement Requirements
4. Scoring
5. Contacts and Acknowledgements
6. References

Appendix A: DEF Placement Submission Procedure

Appendix B: Design and Technology Rules

Appendix C: Floor Plans for the New Benchmarks  
and DEF Region Syntax

# 1. Motivation

---

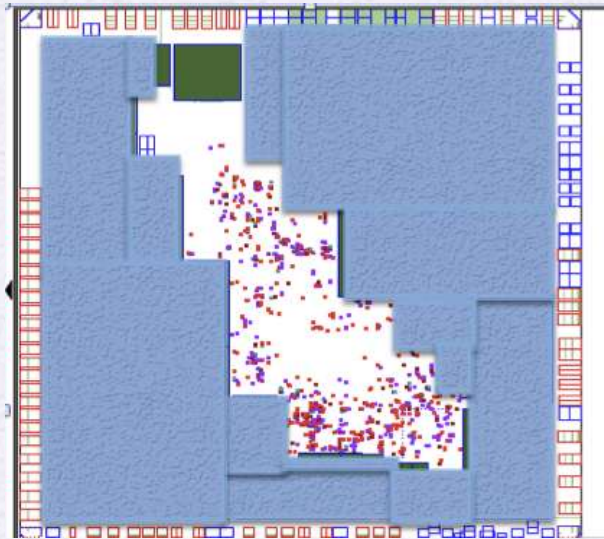


# Motivation

- Increasing complexity of design rules
  - miscorrelation between global routing and detailed routing
  - traditional placement approaches rendered inadequate
- Placement constraints impacting routability
  - Floorplan: irregular placeable area, narrow channels between blocks
  - Design rules: min-spacing, pin geometry, edge-type, and end-of-line
  - Maximum density limit constraints to allow further optimization – **NEW!**
  - Voltage regions and similar region placement restrictions – **NEW!**
- Example routability challenges for placement
  - Netlist: high-fanout nets, data paths, timing objectives
  - Routing: non-default rules, routing layer restrictions and blockages

# Example of Global Routing vs. Detail Routing Miscorrelation

Global routing congestion map



Final DRC violations



	X	Y	Via	Total
Edge Count	1267068	1267137	2115090	4649295
Overflow Edges	6	0	0	6
Overflow as %	0.000129052	0	0	0.000129052
Worst	2	1	0.761905	2
Average	0.200374	0.259198	0.0434537	0.108448
Overflow Nodes	1184	48	-1	1232
Wire Length	1.24525e+11	1.21068e+11	3.85303e+06	2.45593e+11

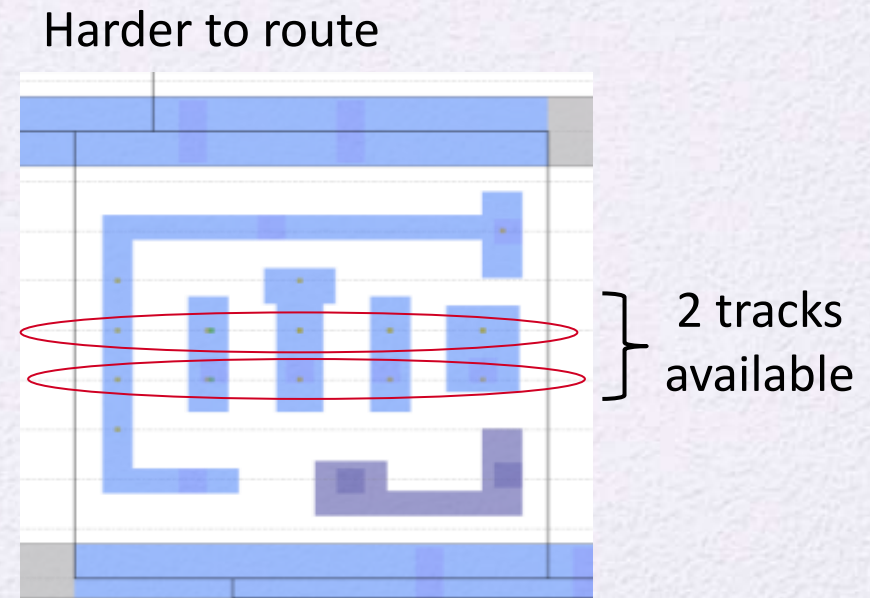
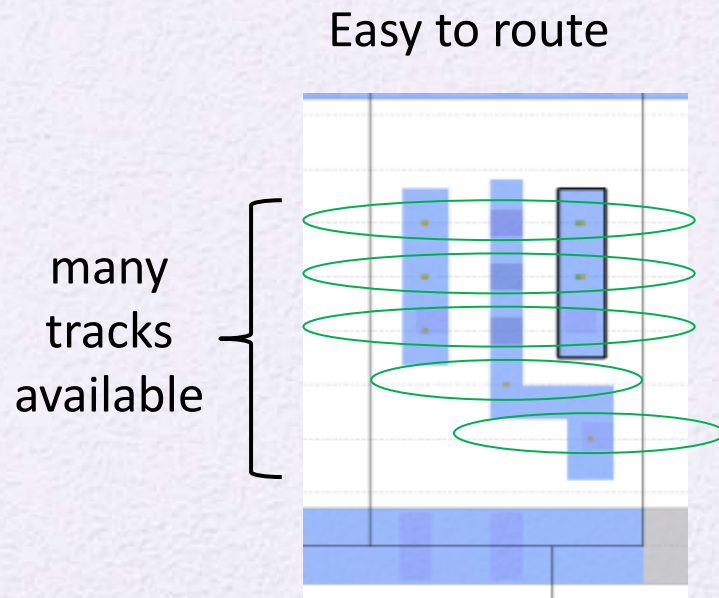
Final Routing (336)
DRC (166)
short (137)
min_hole (1)
min_diff_space (5)
cut_size (21)
cut_min_space (1)
cut_number (1)

- Contests prior to ISPD 2014 have not checked detailed routability!



# Place and Routing Challenges

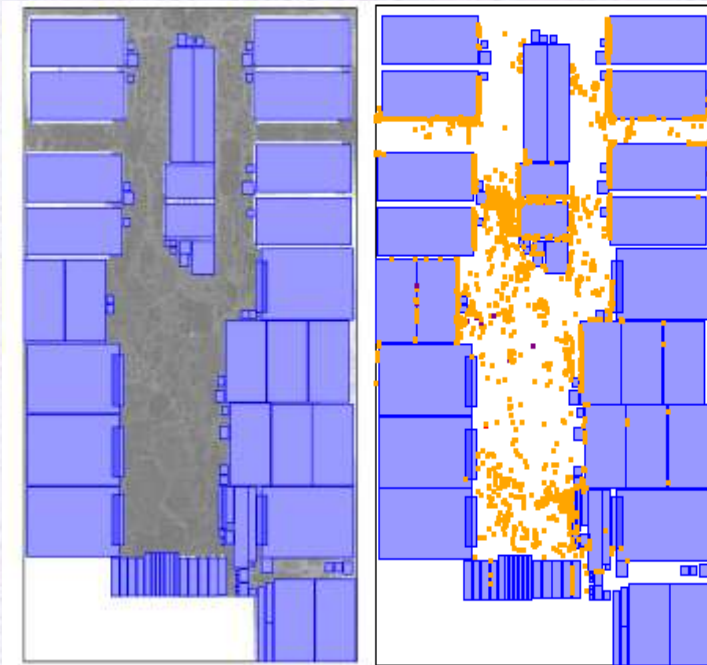
- Dense metal1 pins, pin accessibility, power/ground grid
- Complex DRC rules: cut space, minimum metal area, end-of-line rules, double patterning rules, etc.
- Challenging to pre-calculate routable combinations



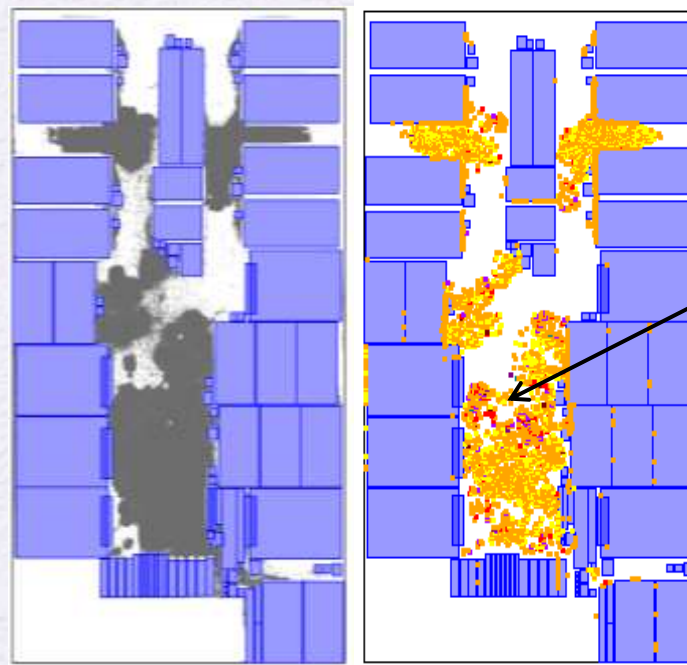
# Why impose density limit constraints?

- Cell spreading is needed for timing optimization, as cell sizing and buffering will increase area usage
- Can also help reduce routing congestion

**mgc\_superblue11 placement and global routing congestion**



with even spread, 65% density limit,  
detail routed wire length 53.6m



with 95% density limit,  
detail routed wire length 46.3m

significantly  
worse  
routing  
congestion

## 2. Benchmark Suite

---



# Benchmark Sources

- There are 16 designs in this year's contest
- They are based on designs originally provided by Intel in the ISPD 2013 gate sizing contest and by IBM in the DAC 2012 routability-driven placement contest
- They are adapted from the 2014 ISPD Detailed Routing-Driven Placement Contest's Benchmark Suites A and B
  - 5 of the 16 designs are the same as in 2014 but with an added maximum density limit.

# Additions to benchmarks this year

- **Fixed macro blockages for placement and routing with narrow “channels”** in between to simulate top-level placement and routing problems
- **Fence placement regions** have been added to simulate voltage region and similar placement restrictions
  - All cells assigned to a region must be placed within it, no other cells may be therein
  - A region may be disconnected, consisting of several non-abutting rectilinear regions
- Added a **maximum density limit** to avoid placements that are not amenable to timing optimization in a “place-and-route” flow
  - This is needed to reserve space for cell sizing and buffering
  - Some submitted 2014 ISPD Placement contest solutions had local area utilization of 100% to minimize the wire length metric
  - **Penalty to wire length score if the density limit is violated!**

# Modifications to ISPD 2013 gate-sizing benchmark designs

- Adapted five designs from the ISPD 2013 suite with a 65nm cell library
- Added sub-45nm design rules (see Appendix B): edge-type, min-spacing, end-of-line, non-default rules (NDRs) for routing
- Pin-area utilizations per cell of about 20%
- L-shaped output pins on 8% of cells in 2 designs, and 2% of cells on 1 design
- Cells were downsized to minimum area
- One cell output pin on M2 to check ability to avoid power/ground rails
- Five routing layers are available: M1, M2, M3, M4, and M5
  - M5 is not allowed for mgc\_fft\_2 – **NEW!**
- M1 is only for vias to metal1 pins, & is otherwise not allowed for routing
- Added **macros with narrow channels as place-and-route blockages**, and enlarged the floorplan footprints from ISPD 2014 contest – **NEW!**
- Added **fence regions**: e.g. single-disconnected region in mgc\_edit\_dist\_a, and three non-rectangular regions in mgc\_matrix\_mult\_c – **NEW!**
- Added blockages to show how to simplify placement, e.g. mgc\_fft\_b – **NEW!**



# Modifications to the DAC 2012 routability benchmark designs

- Adapted three designs from the DAC 2012 suite (mgc\_superblue11, 12, & 16)
- Added 28nm design rules (see Appendix B)
- Pin-area utilizations per cell of about 3%
- All pins are rectangular (no L-shaped pins)
- Cells were left at their original sizes
- Seven routing layers are available: M1, M2, M3, M4, M5, M6, and M7
- M8 is allowed on mgc\_superblue16 to reduce routing difficulty – **NEW!**
- Fence regions were added – **NEW!**
  - Four disconnected fence regions in mgc\_superblue11\_a
  - One disconnected fence region and one non-rectangular fence region in mgc\_superblue16\_a

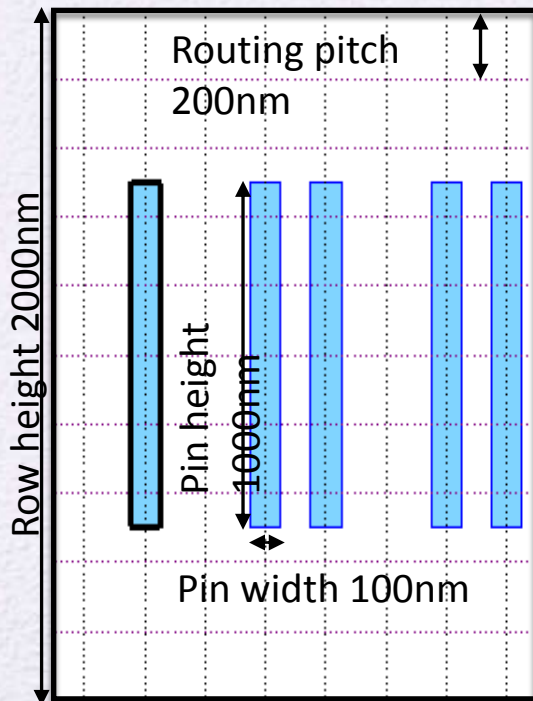
# Standard Cell Libraries

## for Our Benchmarks

**mgc\_edit\_dist, mgc\_des\_perf, mgc\_fft,  
mgc\_pci\_bridge32, & mgc\_matrix\_mult:**

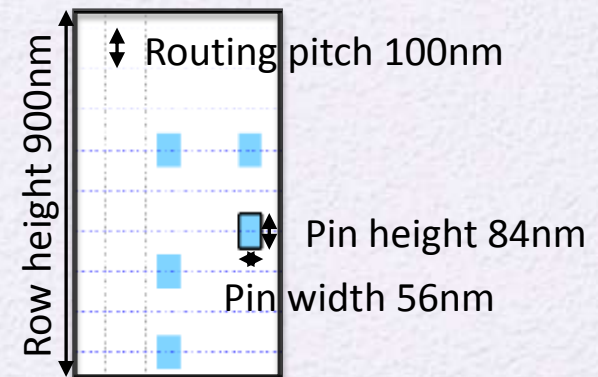
- 65nm technology
- Routing pitch 200nm
- 10 routing tracks per cell row
- All standard cells are single-row high

**Typical  
65nm  
standard  
cell**



**mgc\_superblue11\_a, 12, and 16\_a:**

- 28nm technology
- routing pitch 100nm
- 9 routing tracks per cell row
- All standard cells are single-row high



**Typical 28nm  
standard cell**

# Power/Ground (PG) Mesh

- Dense PG meshes have been inserted in all benchmarks adding to routing difficulty and increasing realism
- Each routing layer has uniformly spaced PG rails parallel to its preferred routing direction
- Rail thickness is constant on each layer but varies by layer
- PG routing-track utilization varies across layers and designs

Suite A metal layer	M1	M2	M3	M4	M5
PG routing track utilization	11%	6%	27%	24%	30%

mgc_superblue11, 12, & 16	M1	M2	M3	M4	M5	M6	M7
PG routing track utilization	0%	1%	5%	8%	5%	9%	5%



# Retained Benchmark Characteristics

- These four designs are retained from the 2014 ISPD Placement contest with the addition of a maximum density limit constraint.
- The maximum density limits are shown in green font – **NEW!**

Design	# Macros	# Cells	# Nets	# Fence Regions	# Primary Inputs & Outputs	%Area Utilization		Density Limit %
						Standard Cells	Standard Cells & Macros	
mgc_des_perf_1	0	112,644	112,878	0	374	90.6	Same	90.6
mgc_fft_1	0	32,281	33,307	0	3,010	83.5	Same	83.5
mgc_fft_2	0	32,281	33,307	0	3,010	49.9	Same	65.0
mgc_matrix_mult_1	0	155,325	158,527	0	4,802	80.2	Same	80.2
mgc_superblue12	89	1,286,948	1,293,413	0	5,908	44.0	57.0	65.0

**Note:** the number of nets excludes the two power/ground nets, vdd and vss.

# New Benchmark Characteristics

- These eleven designs incorporate the new modifications (shown in **green** font) applied to the 2014 ISPD Benchmark designs

Design	# Macros	# Cells	# Nets	# Fence Regions	# Primary Inputs & Outputs	%Area Utilization		Density Limit %
						Standard Cells	Standard Cells & Macros	
mgc_des_perf_a	4	108,288	110,281	4	374	56.7	71.7	56.7
mgc_des_perf_b	0	112,644	112,878	12	374	56.3	49.7	56.3
mgc_edit_dist_a	6	127,413	131,134	1	2574	54.1	61.6	54.1
mgc_fft_a	6	30,625	32,088	0	3,010	28.5	74.0	50.0
mgc_fft_b	6	30,625	32,088	0	3,010	30.9	74.0	60.0
mgc_matrix_mult_a	5	149,650	154,284	0	4,802	44.9	76.8	60.0
mgc_matrix_mult_b	7	146,435	151,612	3	4,802	34.2	72.6	60.0
mgc_pci_bridge32_a	4	29,517	29,985	4	361	64.0	50.8	64.0
mgc_pci_bridge32_b	6	28,914	29,417	3	361	27.3	50.6	27.3
mgc_superblue11_a	1,458	925,616	935,613	4	27,371	35.1	73.0	65.0
mgc_superblue16_a	419	680,450	697,303	2	17,498	50.2	73.9	55.0

# **3. Placement Requirements**

---



# Submitted DEF

## Placement Requirements

- You are expected to provide a DEF file containing the output of your placer.
- Placement legalization is recommended but not required.
- The file name must be gzipped and prepended with the design name (e.g. mgc\_fft.def.gz).
- Please modify the **COMPONENTS** section of the provided **floorplan.def** file to place all **UNPLACED** cells with appropriate placement locations from your placer.

Add the **bottom left coordinate (BLC)** of each placed cell and change

“+ **UNPLACED**” tag to “+ **PLACED ( <x\_BLC> <y\_BLC> ) <cell orientation>**”

Example:    - u1 INVX1 + **PLACED ( 60000 20000 ) N ;**

- Changes other than to the **COMPONENTS** disqualify the submitted placement.

# Evaluation Metric

- Submitted DEF placement solutions will be evaluated by the quality of their detailed routes in Mentor Graphics' Olympus-SoC™ place and route tool
- A placement checker will check the validity of placed designs. If the submitted DEF placement is invalid, you will receive an e-mail with the respective errors
- Valid placements will be **legalized, routed, and scored** based on cell legalization perturbations, maximum utilization violations, detail routed wire length, routing violations, and design-rule check (DRC) violations
- **Note 1: run time will be part of the final evaluation metric,** even though it is not part of the incremental evaluations.
- **Note 2:** Excessive memory usage will be penalized. Memory limits for this suite will be posted later.
- **Note 3:** The contest organizers may change these metrics if necessary for a fair evaluation, in particular density overflow weighting may be modified.

# DEF Placement Validity Checker

- **A Perl script shall check that the submitted DEF placement meets the following minimum requirements:**
  - All cells must be placed within the floorplan boundary
  - No cells may be added, removed, or changed
  - Locations of fixed cells and I/O pins must not change
  - Floorplan boundary must not change
  - Net connections must not change
    - Connectivity can be omitted from the placed DEF
- **Placed DEF files that have any of these problems will not be evaluated.**
- A summary of these errors will be emailed to the contestant.  
**The script is provided to contestants to check before submission.**



# Placement Legalization

Olympus-SoC™ placement legalization will fix any of these issues in submitted DEF files:

- **Edge-type violations and overlaps** between cells or with blockages
- **Cells not aligned** on the standard cell rows
- Cells with **incorrect orientation**
- Cell pins that **short to the PG mesh**
- **Blocked cell pins** that are inaccessible due to the PG mesh
- **DRC placement violations** between standard cells
- Cells outside their **fence region** will be moved inside it, cells not assigned to a fence region will be moved outside it – **NEW!**

Significant cell displacement in legalization is penalized ( $S_{DP}$  score), so we recommend minimizing such issues in your submission.

## 4. Scoring

---

# Final Placement Score

$$S = S_{DP} + S_{DR} + S_{WL'} + S_{CPU}$$

- Each of the following categories contribute up to 25 points to the total score  $S$  out of 100 for a benchmark:
  1.  $DP$ : average **legalization displacement** in standard cell row heights of the 10% most displaced of all cells
  2.  $DR$ : square root of the weight sum of **detailed-routing violations**
  3.  $WL'$ : **detail-routed wirelength** **scaled by a density-limit violation penalty – NEW!**
  4.  $CPU$ : **total runtime** of global placement, legalization, and routing
- A lower score is better.
- **Placements are invalid and receive the maximum score  $S = 100$  if  $DP \geq 25$ ,  $CPU \geq CPU_{max}$ , or GR edge overflow is more than  $GR_{edge\_max}$ .**
  - $GR_{edge\_max}$  overflow will be determined by design and will be included in the output report



# Wirelength scaling by density limit violations

- The bins to analyze placement density are 8x8 standard cell row heights
- The available area of bin  $b$  is  $white\_space(b)$
- For regions, the density limit is  $\max\{density\_limit, region\_utilization\}$
- The overflow for a bin  $b$  is calculated from the area of movable cells  $c$  in that bin,

$$bin\_overflow(b) = \max\left\{0, \left(\sum_{c \in b} area(c \cap b)\right) - white\_space(b) \times density\_limit\right\}$$

$$total\_overflow = \sum_{b \in Bins} bin\_overflow(b)$$

- Total overflow  $f_{of}$  as a fraction of the total cell area:

$$f_{of} = \frac{total\_overflow}{\sum_{c \in Cells} area(c)}$$

- Scaled wirelength,  $WL' = WL \times (1 + f_{of})$

# Detailed routing violations $DR$

- The weighted sum of detailed routing violations  $DR$  is computed from the number of violations  $v_i$  of routing violation type  $i$  and weight  $w_i$  in the table below

$$DR = w_1v_1 + w_2v_2 + w_3v_3 + w_4v_4$$

Design Violation Type	Weighting $w_i$
Routing open	1.0
Routing blocked pin	1.0
Routing short	1.0
Design rule check (DRC) violation	0.2

# Category score normalization

- Each category score except *DP* is normalized by the median unscaled score taken over all contestants' placements for the given benchmark
- Each normalized category score is scaled to the interval [0, 25]
  - Affine scaling  $f_{\text{aff}} : [a, b] \rightarrow [0, 25]$  is used for all categories except *DR*:  
 $f_{\text{aff}}(t) = 25(t - a)/(b - a)$ , where  $a \leq t \leq b$
  - **The square root of the raw *DR* score is taken before affine scaling, as routing and DRC violation counts vary significantly**



# **5. Contacts and Acknowledgements**

---

# Contact Information

- Please e-mail any benchmark-related questions to **ispd2015contest@gmail.com**
- Contest organizers from Mentor Graphics:
  - Ismail Bustany – contest chair
  - David Chinnery
  - Joseph Shinnerl
  - Vladimir Yutsis
  - Ivan Kissiov
  - John Jones
  - Clive Ellis

# Acknowledgements

We wish to thank the following colleagues for valuable insights and help (in alphabetic order):

- Chuck Alpert
  - Yao-Wen Chang
  - Chris Chu
  - Kevin Corbett
  - Nima K. Darav
  - Azadeh Davoodi
  - Igor Gambarin
  - John Gilchrist
  - Andrew B. Kahng
  - Alexander Korshak
  - Shankar Krishnamoorthy
  - Wen-Hao Liu
  - Igor L. Markov
  - Mustafa Ozdal
  - Cliff Sze
  - Liang Tao
  - Alex Vasquez
  - Natarajan Viswanathan
  - Alexander Volkov
  - Yi Wang
  - Benny Winefeld
  - Evangeline Young
- Professor Evangeline Young and her student Wing-Kai Chow generously provided their **RippleDP** detailed placer to the contest.
  - Dr. Wen-Hao Liu generously provided his **NCTUgr** global router to the contest.



## 6. References

---

# References

1. V. Yutsis, et al., “ISPD 2014 Benchmarks with Sub-45nm Technology Rules for Detailed-Routing-Driven Placement”, *International Symposium on Physical Design*, pp. 161-168, 2014.
2. M. M. Ozdal, et al., “An Improved Benchmark Suite for the ISPD-2013 Discrete Cell Sizing Contest”, *International Symposium on Physical Design*, pp. 168-170, 2013.
3. N. Viswanathan, et al., “The DAC 2012 Routability-Driven Placement Contest and Benchmark Suite”, *Design Automation Conference*, pp. 774-782, 2012.
4. G.-J. Nam, et al., “ISPD 2005/2006 Placement Benchmarks”, *Modern Circuit Placement Best Practices and Results*, pp. 3-12, 2007.
5. Si2, Lef/Def Exchange Format Ver 5.3 to 5.7, 2013.  
<http://www.si2.org/openeda.si2.org/projects/lefdef>
6. A. Kennings, N. Darav, and L. Behjat, “Detailed placement accounting for technology constraints”, *International Conference on Very Large Scale Integration*, 2014.
7. C.-K. Wang, et al., “Closing the Gap between Global and Detailed Placement: Techniques for Improving Routability”, *International Symposium on Physical Design*, 2015.

# **Appendix A:**

## **DEF Placement**

### **Submission Procedure**

---



# Industry standard data format

Each benchmark has five input files:

- **floorplan.def**: with unplaced standard cells, net connectivity, fixed I/O pins and fixed macro locations, and routing geometry
- **cells.lef** (physical LEF): detailing physical characteristics of the standard cells including pin locations and dimensions, macros, and I/Os
- **tech.lef** (technology LEF): detailing design rules, routing layers, and vias
- **design.v**: flat netlist with cells, I/Os, & net connectivity (same as in floorplan)
- **placement.constraints**: text file specifying density limit % (**non-standard**)

Outputs from contestant's placement tool:

- Globally placed **DEF gzipped file with all standard cells placed**
- No changes allowed in cell sizes or connectivity

The Library Exchange Format (LEF) and Design Exchange Format (DEF) files are specified with version 5.8, but all constructs are from the 5.7 version, detailed here: <http://www.si2.org/openeda.si2.org/projects/lefdef>

# DEF Placement Submission Procedure

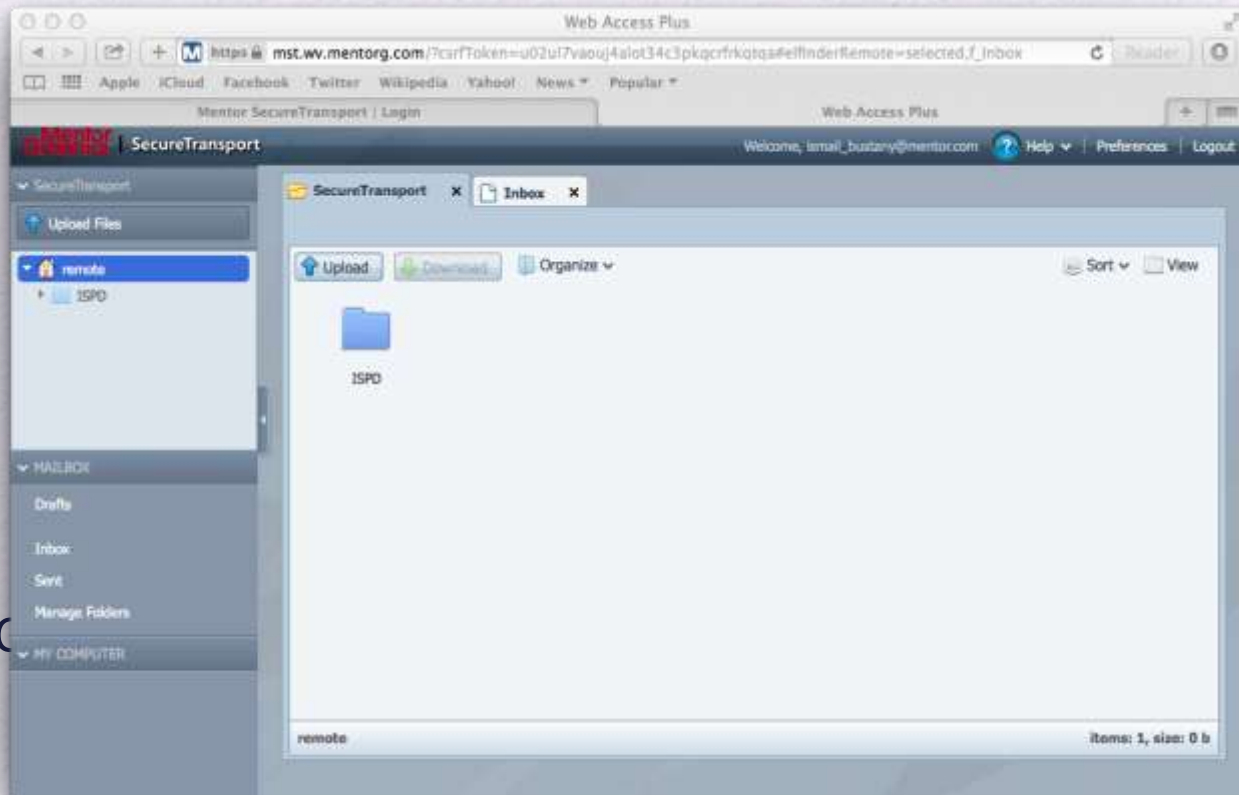
1. Please visit <https://mst.mentorg.com/>
2. Login using your support-net account email and password. If you do not have a support-net account, please e-mail [ispd2014contest@gmail.com](mailto:ispd2014contest@gmail.com).



The screenshot shows a web browser window displaying the login page for Mentor Graphics SecureTransport. The page has a dark blue header with the Mentor Graphics logo and the text "SecureTransport". Below the header, the word "Login" is displayed in white. The main content area is light blue and contains two input fields: "User ID:" with the text "team\_lead@univeristy.edu" and "Password:" with a masked password "\*\*\*\*\*". Below the password field is a link "Forgot Your Password?" with a small blue checkmark icon. A "Log In" button is located at the bottom right of the form.

# DEF Placement Submission Procedure

3. Once logged in, you will see the following screen:

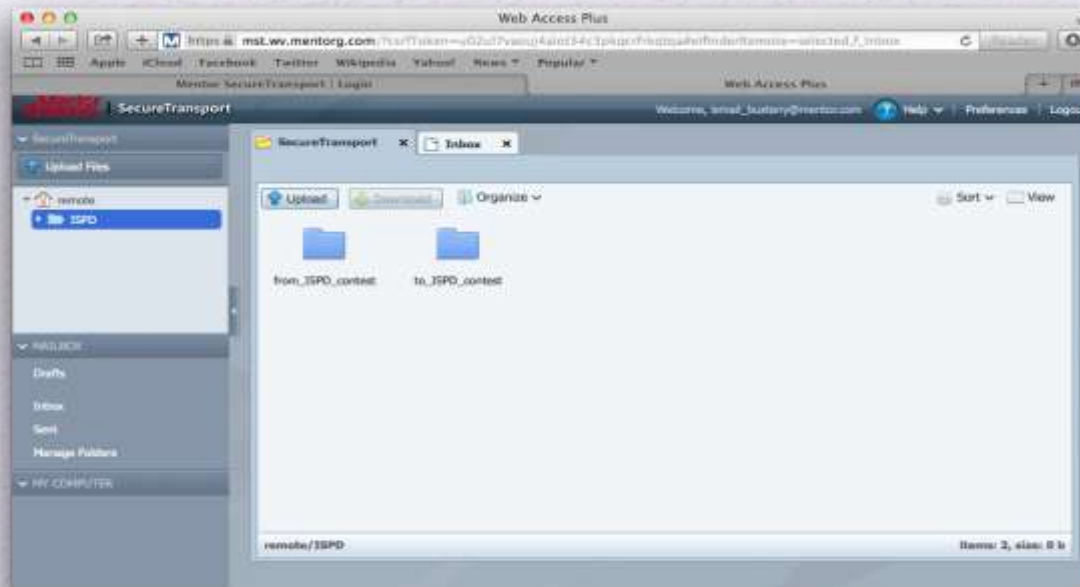


4. C



# DEF Placement Submission Procedure

5. You will see two folders: **from\_ISPD\_contest** and **to\_ISPD\_contest**:



5. Upload your DEF placement to the **to\_ISPD\_contest** folder. **Please use the design name appended by .def.gz (e.g. mgc\_fft.def.gz). Gzip compressed files are required.**

# DEF Placement Submission Procedure

7. Your gzipped DEF placement file will be processed. You will be notified by e-mail once the evaluation result is ready to view.
8. If the placement file is invalid an error log will be copied to the from\_ISPD\_contest folder; otherwise, a tar gzipped output file will be copied there.
9. Upon e-mail notification, please log in to [mst.wv.mentorg.com](http://mst.wv.mentorg.com). You can download a gzipped tar output file in the from\_ISPD\_contest folder.

**Note:** There will be a limit on the number of submissions per day. Currently, it is 8 submissions per day. This may be adjusted depending on the server load. Updates will be posted on the contest website.

# **Appendix B:**

## **Design and Technology Rules**

---



# Introduction to Design Rules

- For 65nm technology and below, many rules are imposed to ensure a printable GDSII mask.
- **The examples provided here are not comprehensive.** They are common on the benchmarks for this contest.
- For the LEF/DEF format specification of design rules, see [www.si2.org/openeda.si2.org/projects/lefdef](http://www.si2.org/openeda.si2.org/projects/lefdef).

# Design rules in physical LEF data

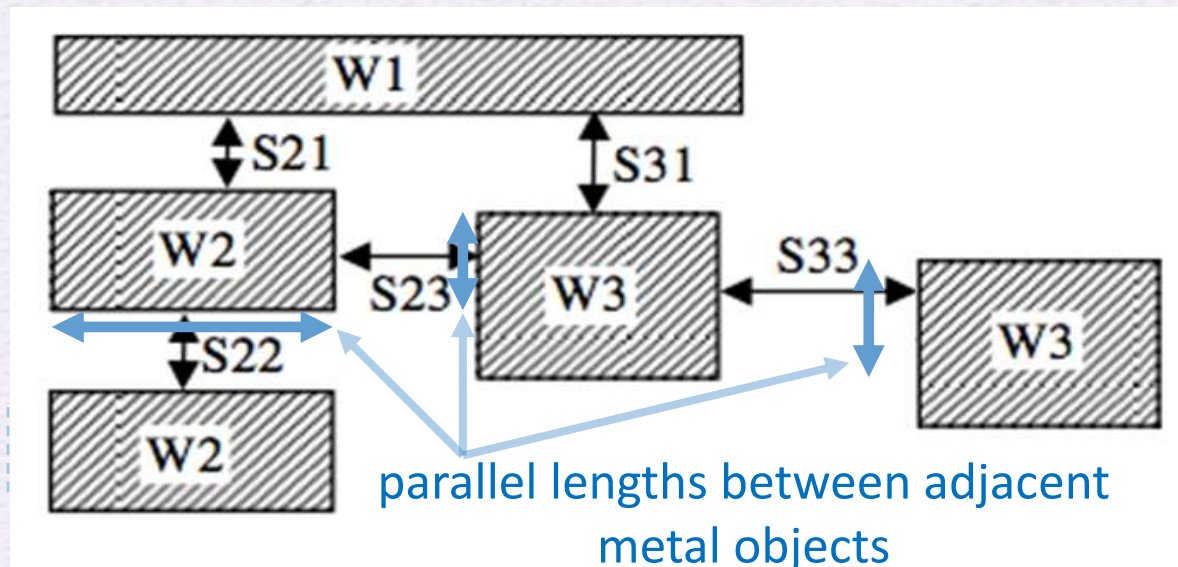
1. Most cell pins are located on metal1 layer.
2. NDR with 2x wire width and 2x wire spacing for nets with fanout > 10.
3. Standard cell ms00f80: driving pin is promoted to metal2 layer to check ability of placement to prevent intersection with PG rails.
4. Standard cell ao22s01: output pin near edge on metal1, but has edge-type constraint with 2x spacing (0.2um).
5. Standard cell oa22f01: Promoted output pin “o” to metal2 and imposed 2x width, 2x spacing, 2-cut vias EM\_NDR.

**This restriction should be observed within 1.0 um (i.e. 5 pitches) of the output pin, afterwards it is switched to the default rule.**

- There are two variants of this rule:
  - I. Double width (0.2um) for pin “o” and edge-type spacing 0.2um assigned to edge next to pin “o”, with EM\_NDR double wire width and double wire spacing.
  - II. Single-width L-shaped pin for “o”.

# Minimum Spacing Rule

- There is a required minimum spacing between any two metal edges.
- The minimum spacing requirement depends on:
  1. The widths of the two adjacent metal objects.
  2. The parallel length between the two adjacent metal objects.



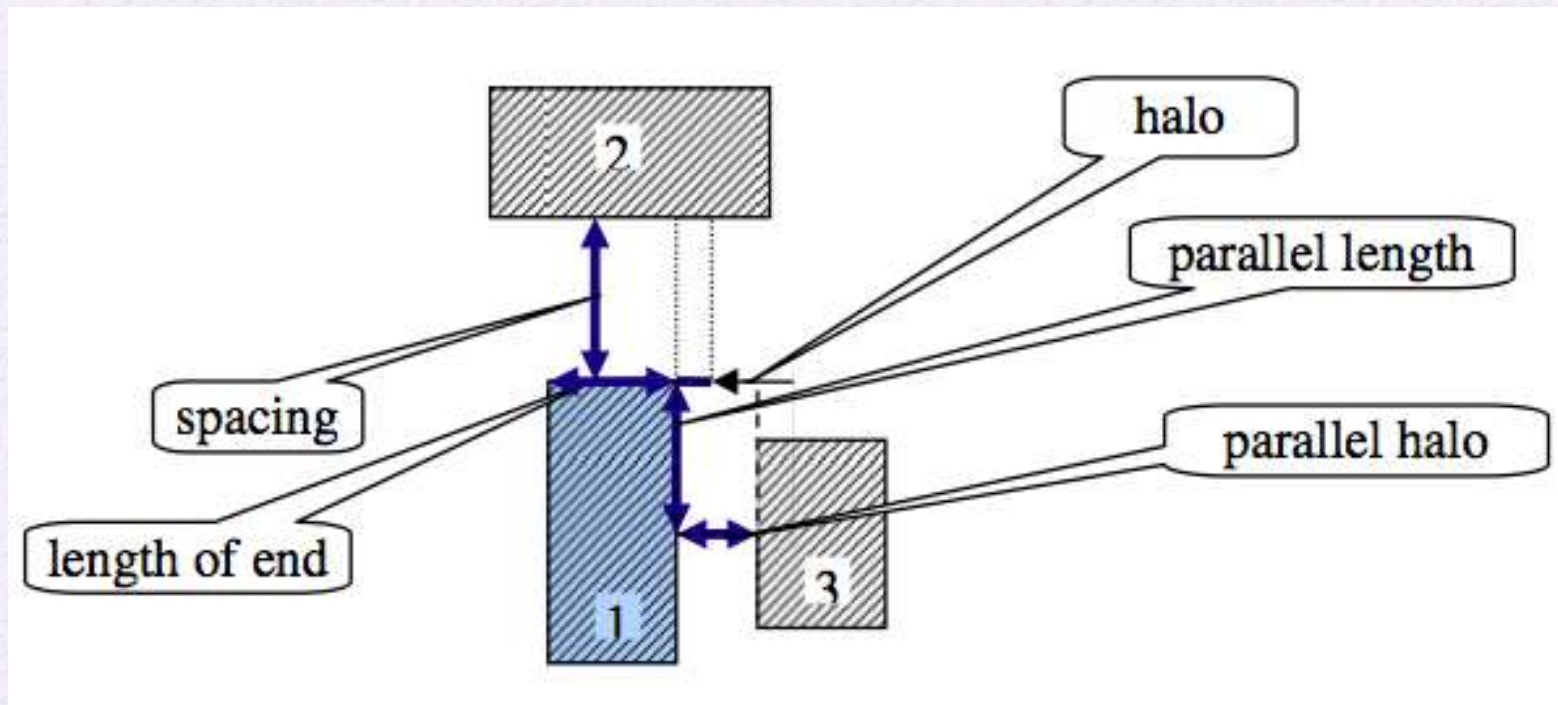


# End of Line (EOL) Rule

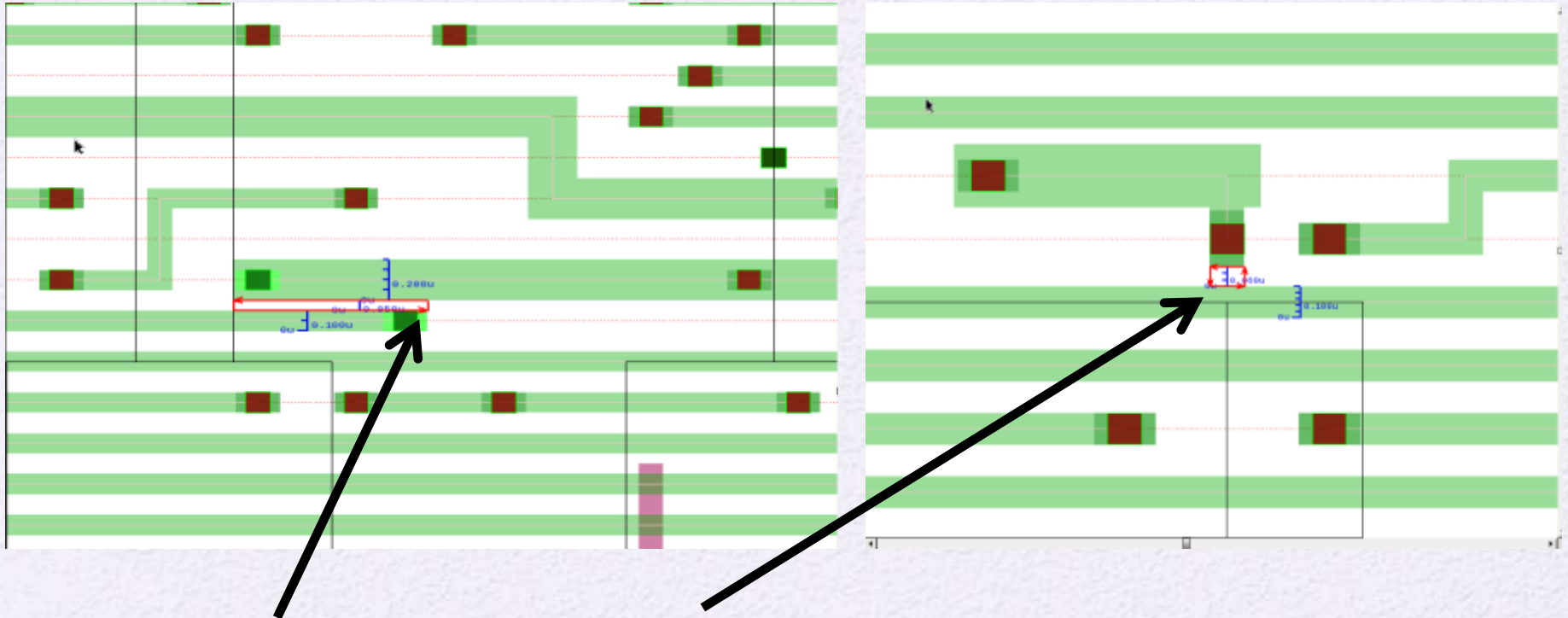
- **EOL is a spacing rule between two objects. However, more than two shapes can be involved, and various distance metrics can be used.**
- A 3-object EOL between the top of object 1 and the bottom of object 2 is illustrated on the next slide.
- EOL is a function of these four parameters:
  - **Length of end:** A minimum width for object 1 to avoid a violation.
  - **Parallel length:** Vertical distance below the top of object 1 within which object 3 will increase the minimum spacing between objects 1 and 2.
  - **Halo:** Area around corner of object 1 where object 2 may trigger EOL rule.
  - **Parallel halo:** Min spacing between object 1 and object 3 to avoid a violation.
    - *The parallel halo is an extra spacing requirement in addition to the EOL spacing.*

# End of Line Parameters

- EOL spacing applied to objects 1 and 2:
  - As object 3 overlaps the parallel length from the top of edge 1, EOL spacing between objects 1 and 2 will be required.
  - Object 3 must remain outside the parallel halo.



# Min Spacing and End-Of-Line Spacing Violation Examples

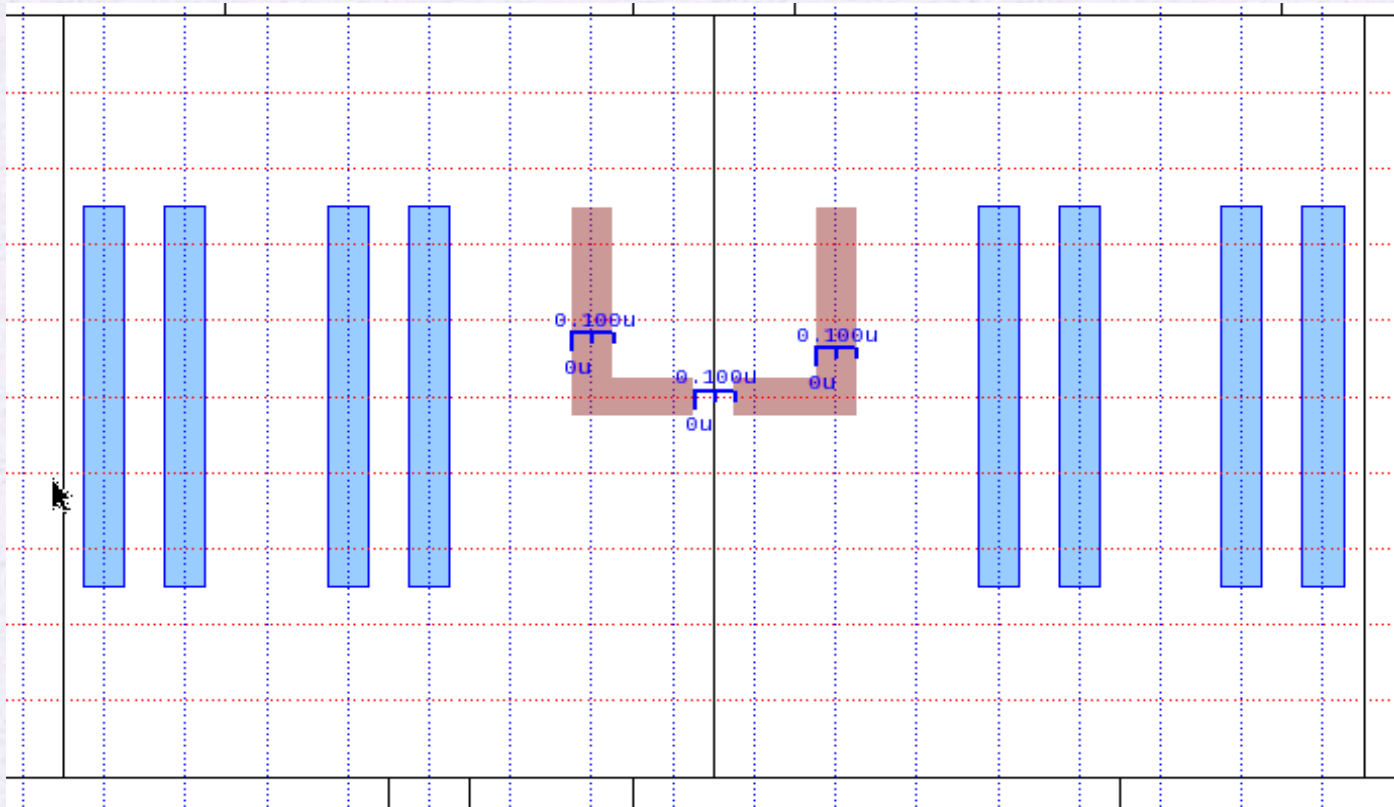


Example **minimum spacing** and **EOL spacing** violations between routing objects within over-congested areas. Most of these violations occur in the vicinity of pins assigned with the EM\_NDR non-default routing rule.



# End-Of-Line Spacing Violation Example

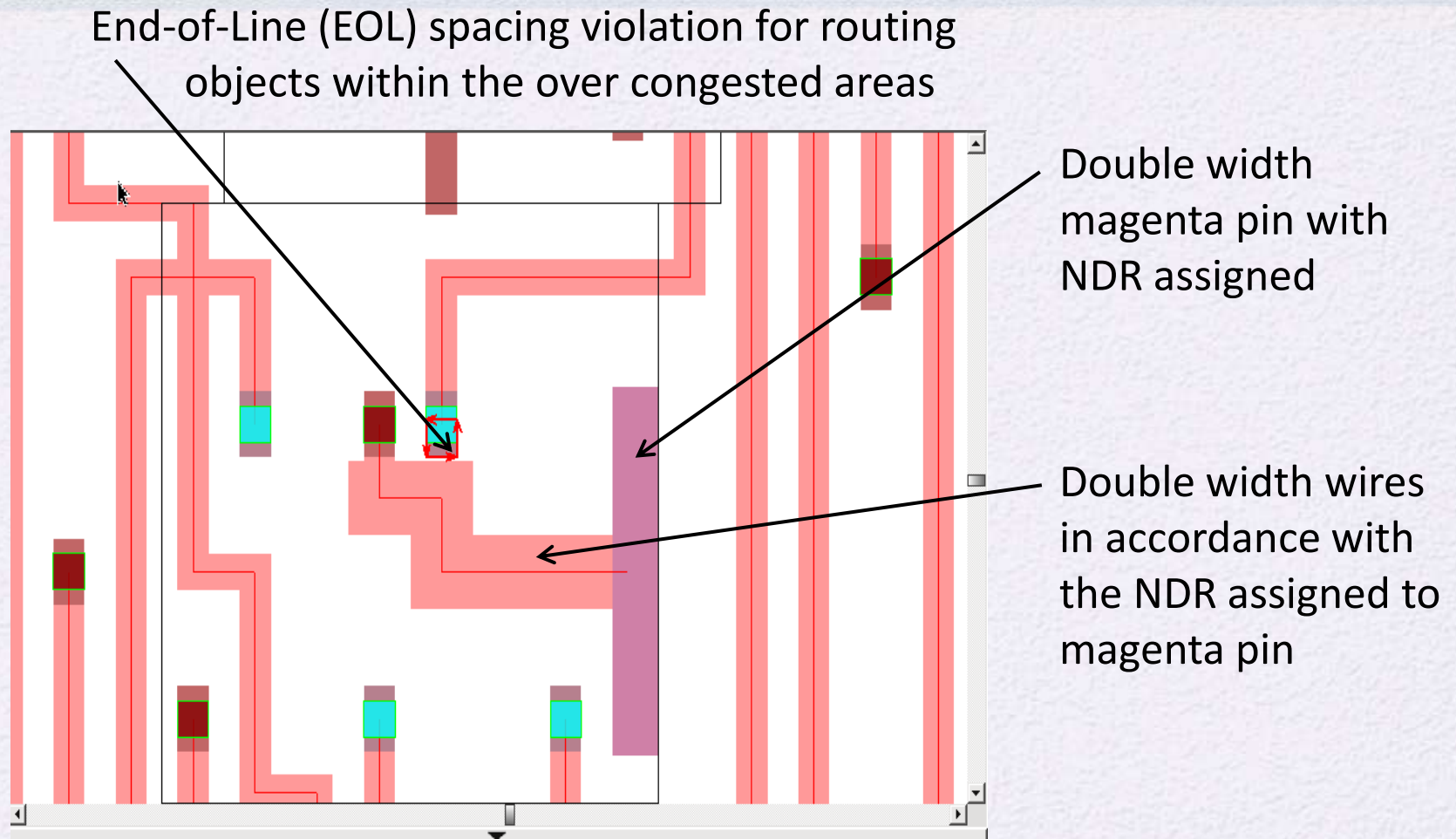
L-shaped pin – EOL spacing violations can occur if two such cells are abutted.



# Non-Default Routing Rule (NDR)

- Non-default routing rules may specify:
  - Increased wire spacing for a net
  - Increased wire width for a net
  - Increased via cut number at selected junctions  
Cut number = number of vias connected to a wire at a single junction
- NDR may be assigned to a cell pin for wires or vias connecting to it
- NDR may or may not accompany increased pin width or specific non-rectangular pins
- NDRs are specified in the floorplan DEF file but may be assigned to a pin in the cell LEF file

# Example End-of-Line Spacing Violation Due to an NDR





# Edge-Type Rule

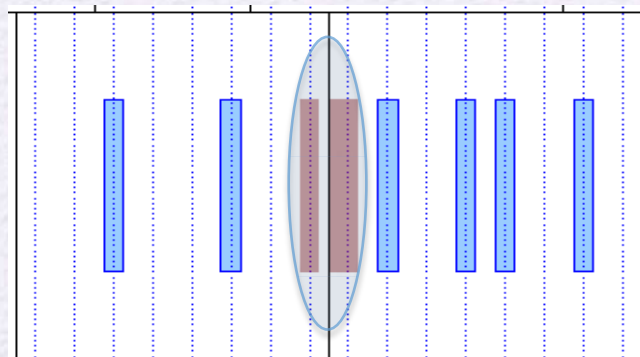
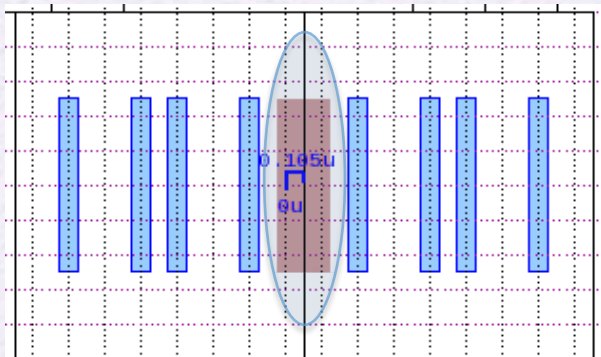
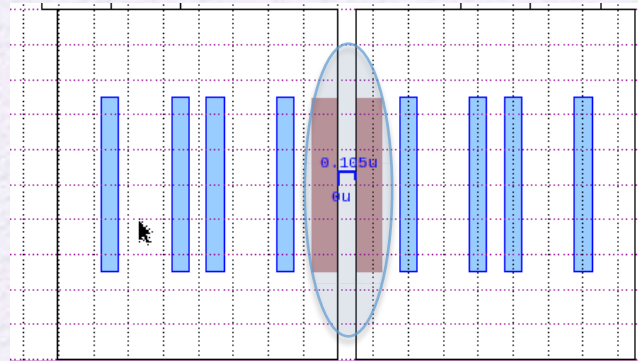
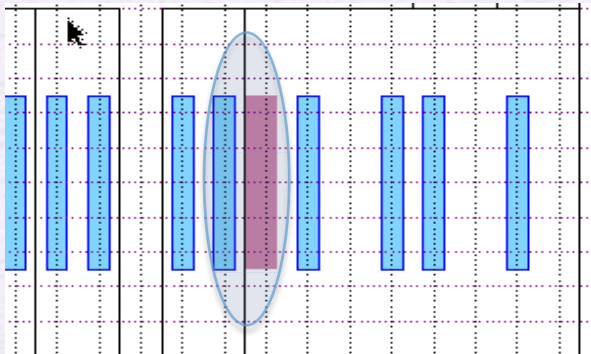
- Each **vertical edge** of a cell may have specified minimum spacings from any other vertical cell edge that can be placed right or left of it.
- They may be for yield, different implant dosages, pin reachability, etc.
- Examples:
  - The **left** edge of every ao22s01 cell must be placed at least 0.400um away from the **left** edge of every other ao22s01 cell.
  - The **left** edge of every ao22s01 cell must be placed at least 0.800um away from the **right** edge of every other a022s01 cell adjacent to it.

# Edge-Type Spacing Violation Examples

**Double width metal2** is used for the red pins.

An **edge-type** double spacing constraint is also enforced at the adjacent cell edge.

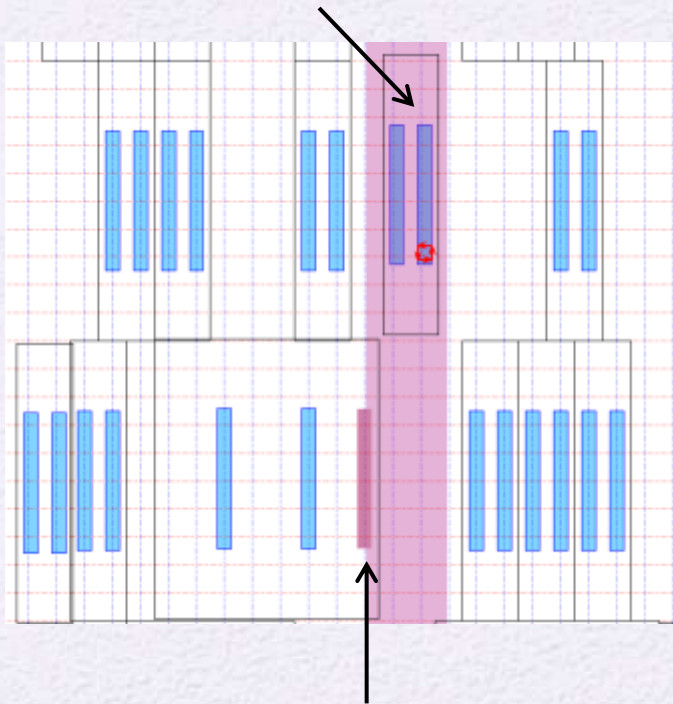
Below are four examples of violations of this:



# Blocked Pin Access Violation Examples

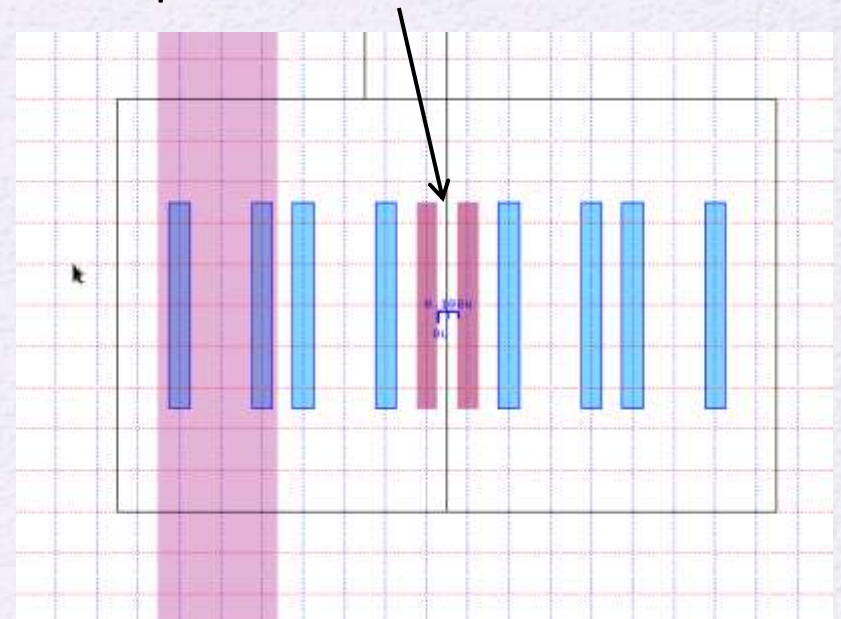
A *blocked pin* cannot be reached by a via or wire without violations.

Metal1 pins under metal2 stripe are not accessible by via1 vias



Metal2 pin overlaps metal2 stripe

Metal2 pins with EM\_NDR assigned are placed too close to each other





# Example spacing rules in tech LEF

LAYER metal2

TYPE ROUTING ;

DIRECTION VERTICAL ;

PITCH 0.200 ;

OFFSET 0.100 ;

WIDTH 0.1 ;

MAXWIDTH 10.0 ;

SPACINGTABLE

PARALLELRUNLENGTH	0.00	0.40	0.46	1.40	4.10
-------------------	------	------	------	------	------

WIDTH	0.00	0.10	0.10	0.10	0.10	0.10
-------	------	------	------	------	------	------

WIDTH	0.30	0.10	0.12	0.12	0.12	0.12
-------	------	------	------	------	------	------

WIDTH	0.46	0.10	0.12	0.15	0.15	0.15
-------	------	------	------	------	------	------

WIDTH	1.40	0.10	0.12	0.15	0.52	0.52
-------	------	------	------	------	------	------

WIDTH	4.10	0.10	0.12	0.15	0.52	1.40 ;
-------	------	------	------	------	------	--------

PROPERTY LEF57\_SPACING "SPACING 0.12 ENDOFLINE 0.14 WITHIN 0.045  
PARALLELEDGE 0.12 WITHIN 0.12 ;" ;

# Example edge-type rules in tech LEF

```
PROPERTYDEFINITIONS
```

```
LAYER LEF57_SPACING STRING ;
```

```
LAYER LEF57_MINSTEP STRING ;
```

```
MACRO LEF58_EDGETYPE STRING ;
```

```
LIBRARY LEF58_CELLEDEGESPACINGTABLE STRING
```

```
"CELEDEGESPACINGTABLE
```

```
EDGETYPE 1 2 0.400
```

```
EDGETYPE 1 1 0.400
```

```
EDGETYPE 2 2 0.000;" ;
```

```
END PROPERTYDEFINITIONS
```

# Min-step, area, and min cut rules in tech LEF

```
PROPERTY LEF57_MINSTEP "MINSTEP 0.1 MAXEDGES 1 ;" ;  
AREA 0.051 ;  
MINIMUMCUT 2 WIDTH 0.400 ;  
MINIMUMCUT 4 WIDTH 0.720 ;  
MINIMUMCUT 2 WIDTH 0.400 LENGTH 0.400 WITHIN 0.820 ;  
MINIMUMCUT 2 WIDTH 2.100 LENGTH 2.100 WITHIN 2.100 ;  
MINIMUMCUT 2 WIDTH 3.200 LENGTH 8.000 WITHIN 5.200 ;
```



# **Appendix C: Floorplans for the New Benchmarks and DEF Region Syntax**

---

# Specific Floorplan Characteristics

- The following slides depict the floorplan characteristics of the eleven new designs in the 2015 ISPD benchmark suite.
- **Please note:** floorplans are not shown to scale!

# Fence Region DEF Syntax

- A **region** is specified in the **floorplan DEF** as one or more rectangles specified by pairs of coordinate points  
(bottom\_left\_corner\_x1 bottom\_left\_corner\_y1)  
(upper\_right\_corner\_x2 upper\_right\_corner\_y2)
- The rectangles might not create a contiguous rectilinear region, i.e. in some cases **a region may be disconnected**
- **Fence** specifies that only the assigned cells must be placed therein

- Example of a disconnected fence region from mgc\_edit\_dist\_a:

```
REGIONS 1 ;  
- r0 ( 305800 92000 ) ( 502400 146000 )  
      ( 305800 214000 ) ( 502400 264000 )  
      ( 305800 322000 ) ( 502400 374000 )  
      ( 305800 434000 ) ( 502400 484000 )  
      ( 305800 536000 ) ( 502400 586000 )  
      ( 305800 640000 ) ( 502400 696000 )  
      + TYPE FENCE ;  
END REGIONS
```



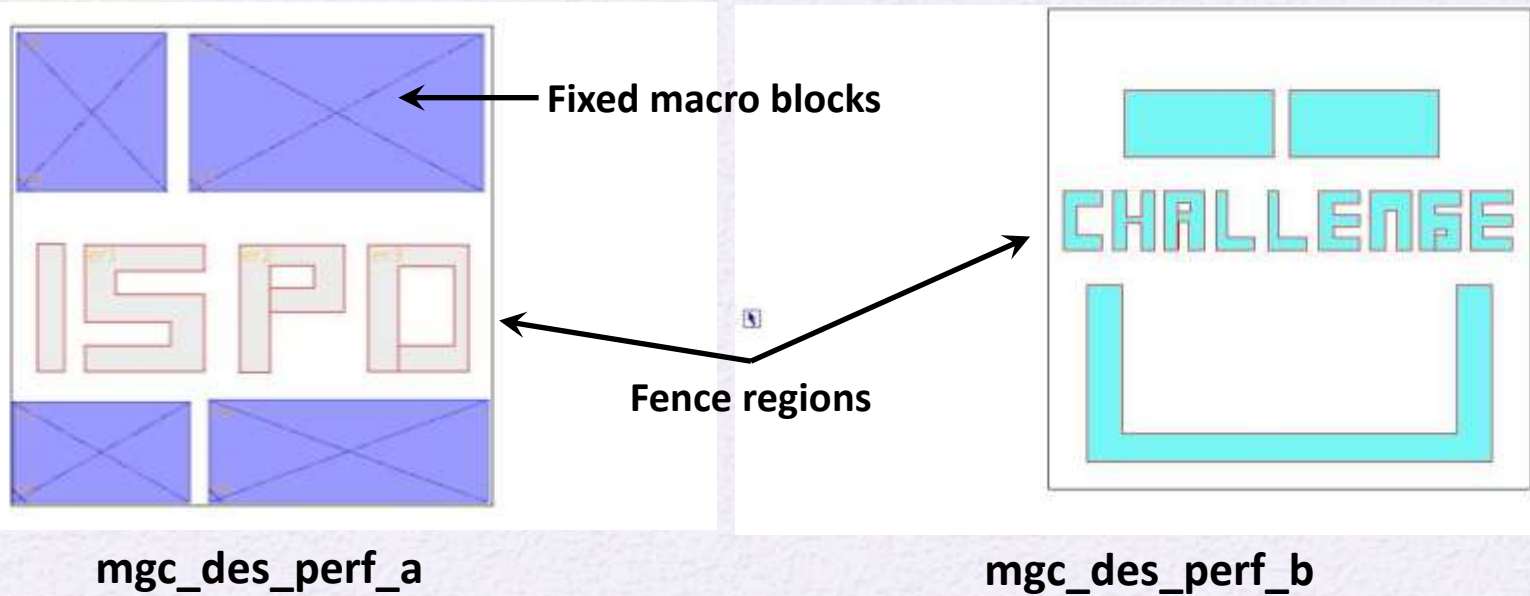
# Groups of Cells Assigned to a Region in DEF Syntax

- A **group** of cells can be specified as all cells matching a given expression, e.g. `h0/*` is all cells with `h0/` as a prefix
- They will be assigned a particular region with  
`+ REGION <NAME>`

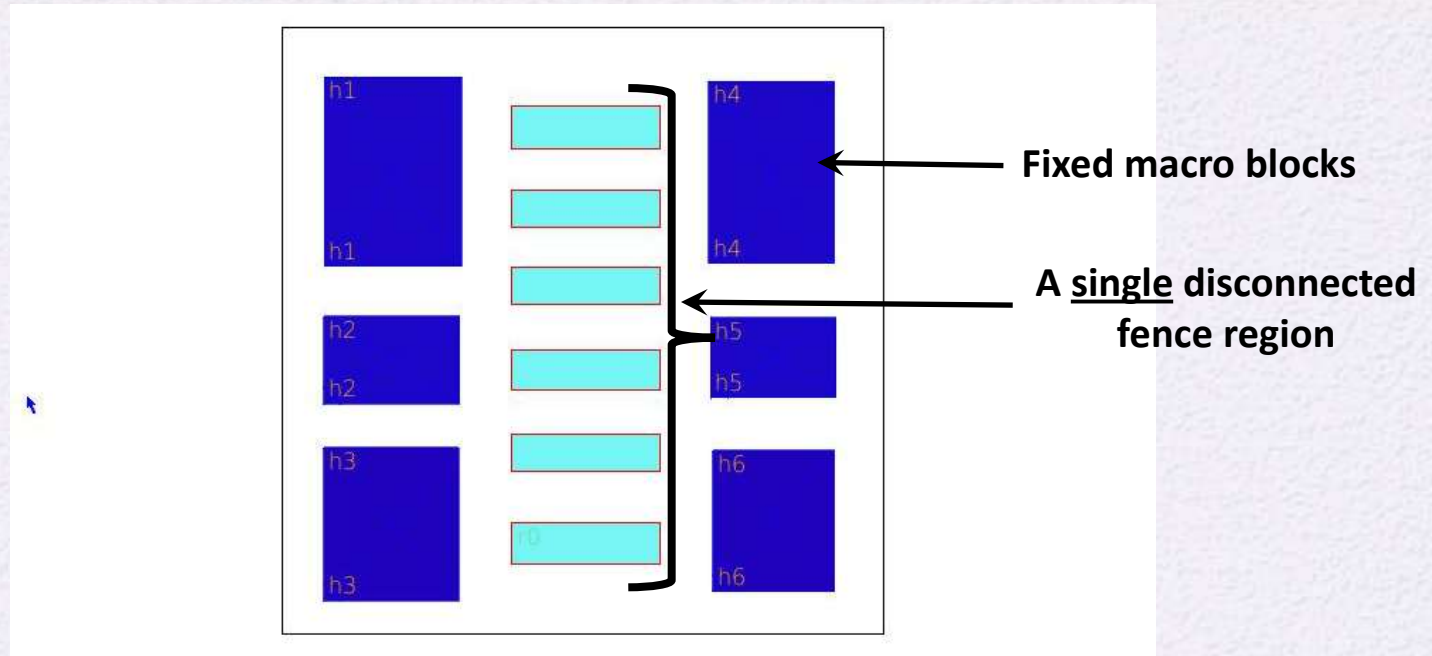
- Example from `mgc_edit_dist_a`:

```
GROUPS 1 ;  
- r0 h0/*  
  + REGION r0 ;  
END GROUPS
```

# mgc\_des\_perf\_a & mgc\_des\_perf\_b



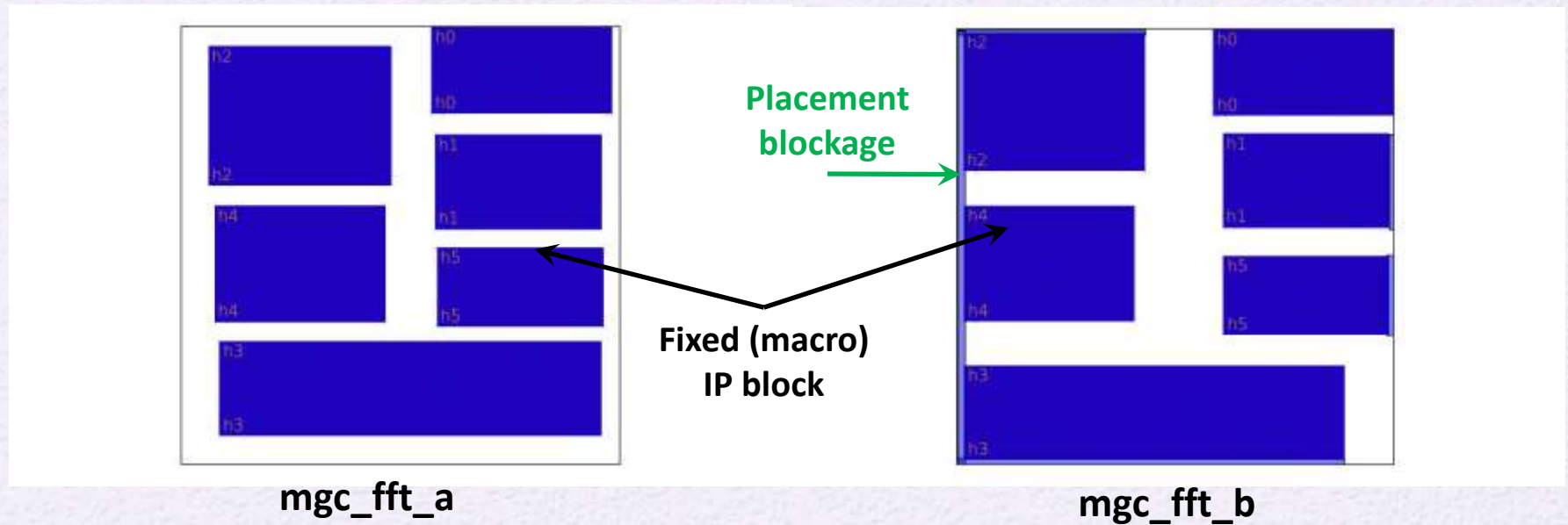
# mgc\_edit\_dist\_a



- A disconnected region may be used for example to intersperse always-on logic within a design
- Cells assigned to that region may be placed in any of those locations

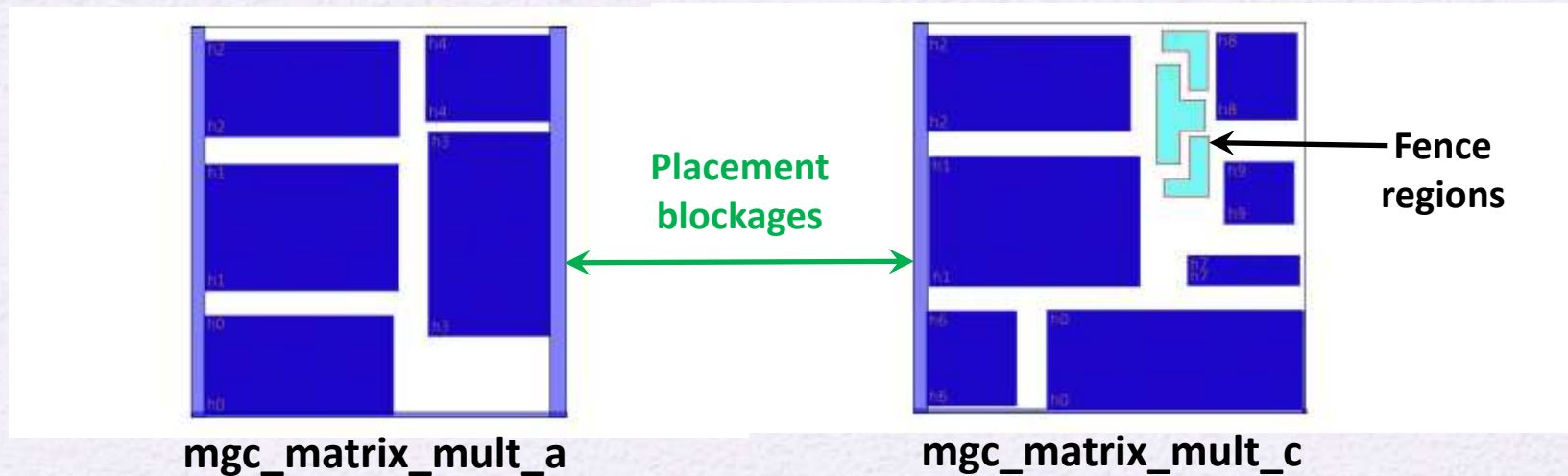


# mgc\_fft\_a & mgc\_fft\_b



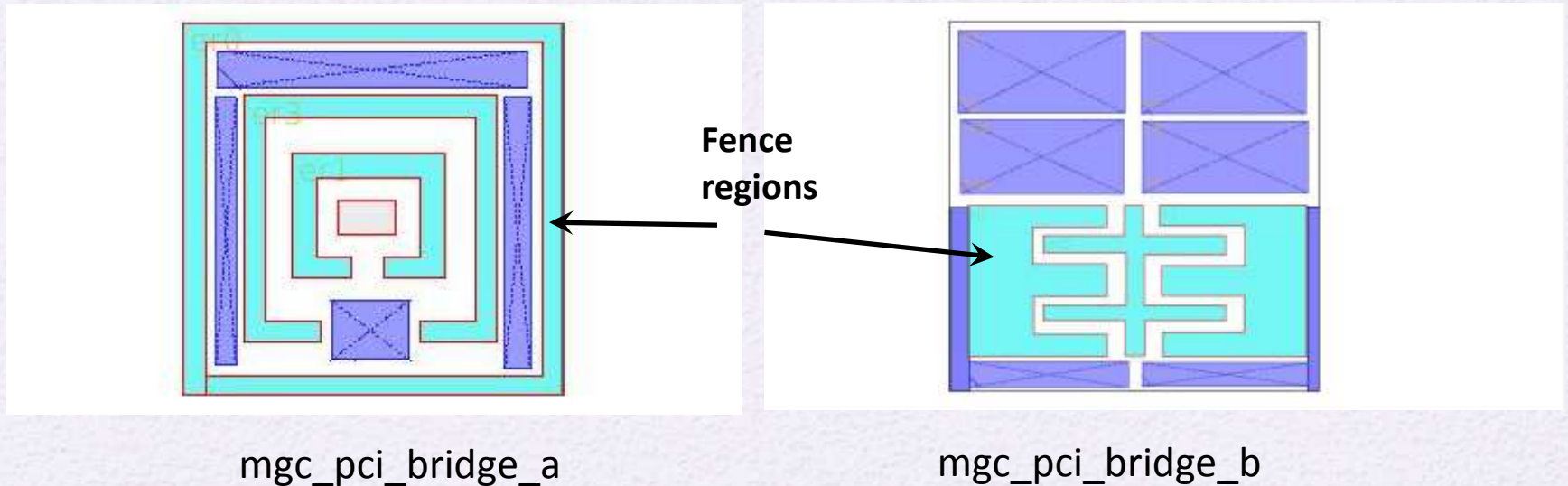
- Placement may sometimes be improved by avoiding narrow regions between the floorplan boundary and macros.

# mgc\_matrix\_mult\_a & mgc\_matrix\_mult\_c



- Floorplan quality significantly impacts placement and routability

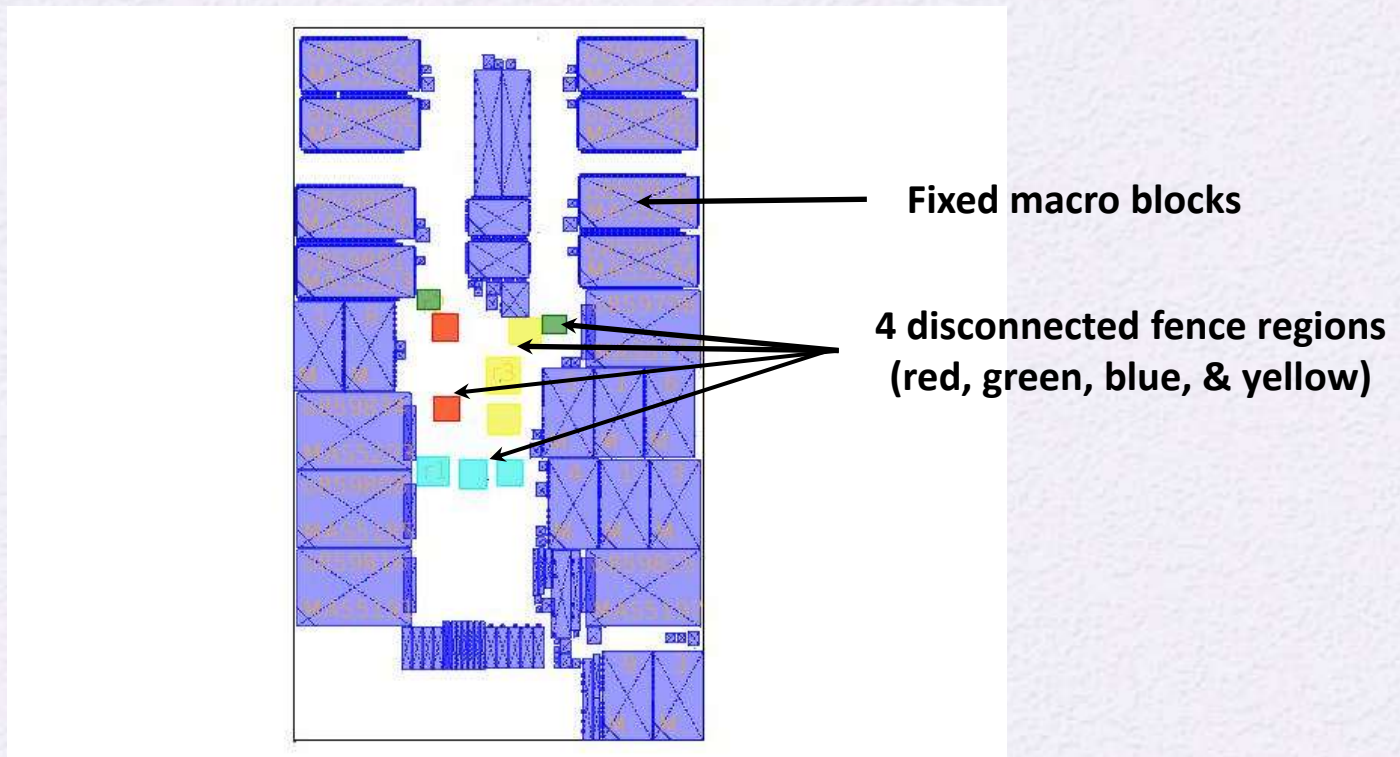
# mgc\_pci\_bridge32a & mgc\_pci\_bridge32b



- The non-rectangular restricted placement regions can be difficult.
- The bottom middle macro blockage in `mgc_pci_bridge32_a` makes this design very difficult if the placement of cells within the narrow channels is haphazard, due to the high routing demands in the narrow channel on either side of the macro.



# mgc\_superblue11\_a



# mgc\_superblue16\_a

