ISPD26 Contest: Post-Placement Buffering and Sizing

Organizing Team: UCSD, Fudan University, POSTECH

Co-Chairs

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Table of Contents

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1. Contest Introduction

Two of the most important approaches for timing optimization after global placement are **repeater insertion** (buffers and inverters) and **gate sizing**. The ISPD26 Contest challenges contestants to develop a **post-detailed placement buffering and sizing tool** under a set of **real-world constraints.**

Real-World Motivation

This open, academic research contest bridges the gap between research methods and real industry flows. Unlike previous contest settings, this contest tries to emphasize physical and electrical constraints seen in practice. Specifically, this contest includes:

- Fixed macros and I/Os
  - Macros occupy large, immovable regions of the layout, often fragmenting available placement space and constraining repeater insertion and gate sizing.
  - Also, I/Os are fixed in our testcases.
- Power delivery network (PDN) blockages
  - The power delivery network (PDN) uses significant routing resources, exacerbating congestion and making DRC-free routability challenging. This makes fixing timing and ERC violations in congested regions more difficult.
- Placement blockages
  - Representing reserved regions, these blockages take away from the usable areas in the placement canvas, and increase legalization difficulty.
- Fixed routing resource
  - The routing track supply is fixed, so the fixing of timing and ERC violations in congested regions, as estimated by the global router, should fit within the available routing track supply.

Together, these constraints significantly complicate post-placement timing optimization. They limit available whitespace, increase local utilization, and raise the difficulty of ensuring legal and congestion-free cell placement.

Scope of the Challenge

The ISPD26 Contest challenges contestants to develop buffering and sizing tools that operate after detailed placement. Their tools are expected to offer the following benefits:

- Physically-aware timing optimization
  - With detailed placement completed, interconnect delays can be estimated more accurately compared to previous physical design stages (e.g., synthesis, floorplanning and global placement). This enables the tool to make effective buffering and sizing decisions for timing optimization.
- ERC violation fixes
  - Electrical rule check (ERC) constraints, such as maximum slew, maximum capacitance, and maximum fanout, need to be addressed at the post-placement stage to ensure that timing analysis is more accurate and requires fewer iterations to fix ERC violations at the signoff stages.
- Legal and congestion-aware insertion
  - Solutions must satisfy all legality constraints, including placement blockages, PDN-induced pin blockage, fixed macros and fixed I/Os. Inserted repeaters and resized gates must be placed in legal, congestion-friendly areas so that global routing finishes within time limits.

This contest is built on top of the OpenROAD [1] infrastructure and provides a controlled, open-source environment for benchmarking and evaluation. To encourage scalability and

innovation, contestants may (but are not required to) leverage **GPU-accelerated** solutions or **modern ML** infrastructure such as PyTorch [2], which have shown strong potential in solving large scale optimization problems in physical design [3][4][5][6][7][8]. The contest's evaluation framework, along with sponsor-provided compute resources that we plan to make available to contest teams who pass certain contest stages, will include GPUs. Nonetheless, the primary objective of this contest remains achieving **better PPA results under real-world constraints.**

2. Contest Objectives

- The contest focuses on post-global placement optimization for better PPA results via:
  - **Repeater (buffers/inverters) insertion**
    - Insert repeaters (buffers/inverters) to fix ERC violations, and to improve timing and power.
  - **Gate sizing**
    - Select appropriate cell variants from the given cell library (differing in drive strength and VT flavor) to balance timing and power.
- Constraints
  - Macros and I/Os are fixed and can not be moved.
  - **PDN and soft placement blockages must be honored.**
    - Within soft blockage regions, only physical/auxiliary cells (Filler cells, Well Tap Cells, Tie Cells and ENDCAP cells) and buffers/inverters are allowed to be placed.
  - Routing track supply is fixed.
  - No netlist restructuring beyond buffer/inverter insertion and sizing.
  - The output netlist must remain functionally equivalent (equivalence will be checked).
  - Setup (late-mode) timing check, single mode with ideal clock.
  - Displacement: logic gates except for repeaters must not be moved too far from their initial legal position. Movement beyond the specified threshold will be penalized.
- The workflow before and after integrating the contestant's tool is shown in Figure 1.
  - ISPD26 Contest workflow steps
    - **Inputs to contestants**:
      - .v file: Debuffered gate-level netlist that is input to OpenROAD global placement
        - Note: The netlist is debuffered with the exception of the I/O buffering added through the ORFS flow. We also run global_placement with timing-driven placement disabled so that no buffers or inverters are added.
      - .def file: post-detailed placement, legalized placement
        - Note: After global placement we run OpenROAD *detailed_placement* and *improve_placement* commands to generate this .def file.
      - .sdc file: Design constraints include clock period, I/O delay etc.
    - **Contestant optimization**: Contestants' tools perform buffering and gate sizing. Their tools must output the modified .v, .def and changelist files (for more details please see output formats).

- **Evaluation flow**: The evaluation flow requires that the submitted placement is legalized and that the netlist is logically equivalent to the input netlist:
  - Legality checks (checkPlacement) and equivalence checks
    - Also: stitch the component placements into the given floorplan .def (including PDN)
  - **If legalized and equivalent**: Directly perform global routing → OpenSTA timing analysis → **report metrics**
  - **If not legalized or not equivalent**:
    - Mark as evaluation failure

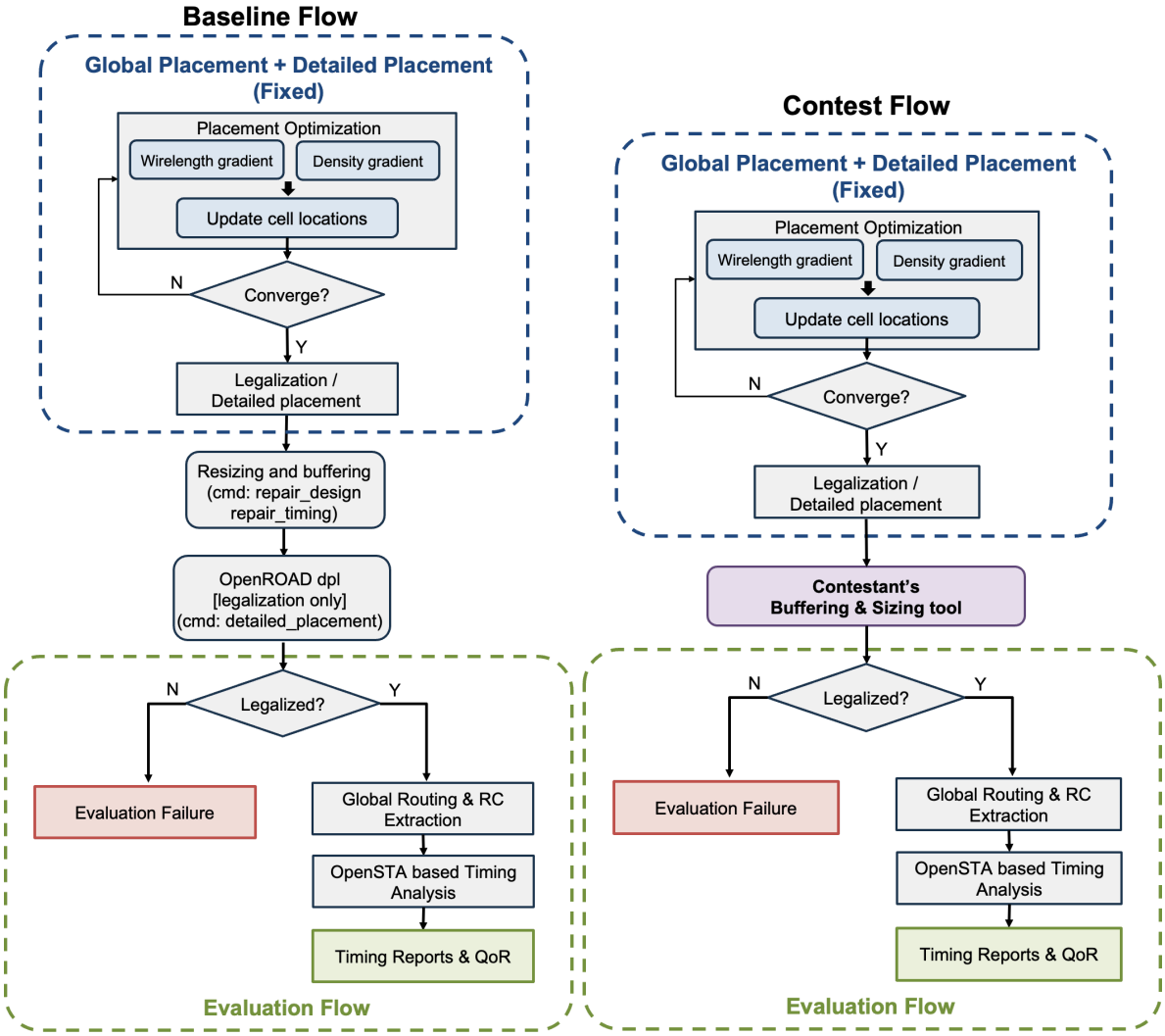

Figure 1. **Left:** Baseline OpenROAD flow. **Right:** ISPD26 Contest flow that integrates the contestant's buffering/sizing tool. Fixed macros, PDN, blockages, and I/O constraints are respected in both flows. The outputs of global and detailed placement are fixed. The evaluation pipeline includes placement legality and equivalence check, global routing, and OpenSTA-based timing and power analysis to report final QoR metrics. **Only the contest integration block (purple) is editable**.

3. Problem Formulation

3.1 Input Formats

Each benchmark will include standard design files in the **ASAP7** technology node. The provided files include:

- **.lef file**: Specifies the physical definitions of the different cells, metal layers, and layout of the design.
- **.lib file**: Library file that consists of the logic description, look-up-tables for delay, slew, and power computation with the area of each cell.
- **.sdc file**: Specifies input port delay and transition, output port delay and capacitance, and specified clock period.
- **.v files**: Debuffered gate-level netlist that is input to OpenROAD global placement.
    - Note: The netlist is debuffered with the exception of the IO buffering added through the ORFS flow.
- **.def file**: post-detailed placement, legalized placement with fixed IOs, macros, PDNs, and placement and routing blockages.

3.2 Output Formats

Your tool must return a legalized placement

- **Modified Verilog Netlist (.v)**: Includes only repeater insertions and cell sizing modifications
- **Updated DEF File (.def)**: Reflects your placement solution (must be legalized)

Note: I/Os can not move. Net names must be preserved. New nets and instances must be named according to the existing OpenROAD convention; see Resizer::makeUniqueNetName [link] and Resizer::makeUniqueInstName [link]. All modifications must preserve netlist functionality (contestants' solutions must pass LEC) and satisfy all hard (non-overlap, legal sites, PDNs, blockages, etc.) design constraints.

3.3 Evaluation: Metrics, Scores, Platforms

3.3.1 Metrics

Contestants' solutions will be evaluated based on global routing quality, runtime efficiency, and legality, using OpenROAD's timing and power analysis infrastructure. Evaluation metrics include

- Post-global route PPA: Compare normalized improvement vs. baseline on setup TNS, dynamic power (internal power + switching power), and leakage power. All results are reported by OpenSTA.
    - Normalized TNS improvement

    - $\Delta_{TNS} = \frac{TNS - TNS_{baseline}}{|TNS_{baseline} + \epsilon|}$
  - Normalized dynamic power improvement
    - $\Delta_{dpower} = \frac{DPower_{baseline} - DPower}{DPower_{baseline}}$
  - Normalized leakage power improvement
    - $\Delta_{lpower} = \frac{LPower_{baseline} - LPower}{LPower_{baseline}}$
  - Combine with weight w_{tns}, w_{dpower} and w_{lpower}
    - $S_{PPA} = w_{tns} * \Delta_{TNS} + w_{dpower} * \Delta_{dpower} + w_{lpower} * \Delta_{lpower}$

- ERC violation penalty
  - Sum of ERC violation values after global routing: slew violation, capacitance violation, and fanout violation
    - $P_{ERC} = w_{slew} * \frac{SlewViolation - SlewViolation_{baseline}}{SlewViolation_{baseline} + \epsilon}$

$$+ w_{cap} * \frac{CapViolation - CapViolation_{baseline}}{CapViolation_{baseline} + \epsilon}$$

$$+ w_{fanout} * \frac{FanoutViolation - FanoutViolation_{baseline}}{FanoutViolation_{baseline} + \epsilon}$$

- Runtime
  - The runtime of the buffering & sizing tool itself
    - $R_{tool} = \frac{t_{tool} - t_{baselineTool}}{t_{baselineTool}}$
      - Where t_{tool} is the runtime of contestants' developed tools, and $t_{baselineTool}$ is the runtime of OR Resizer
  - Total flow runtime (buffering & sizing tool + fixed evaluation flow)
    - $R_{flow} = \frac{t_{flow} - t_{baselineFlow}}{t_{baselineFlow}}$
      - Where t_{flow} is the contestants' total flow runtime, and $t_{baselineFlow}$ is the default (Figure 1, left) total flow runtime
  - Combine with weight $w_{toolRuntime}$ and $w_{flowRuntime}$
    - $R = w_{toolRuntime} R_{tool} + w_{flowRuntime} R_{flow}$
  - Note: Both the tool runtime and flow runtime must not exceed **5 hours**

- Average displacement penalty
  - Average Manhattan displacement per movable cell from its original position

- $P_{dis} = w_{dis} \frac{D_{avg} - D_{baselineAvg}}{D_{baselineAvg} + \epsilon}$

- Global routing overflow penalty
  - **Maximum** O_{max} global routing overflow values after routing (thresholds $O_{max\,Thr}$)
    - $P_{max} = \frac{O_{max} - O_{maxThr}}{O_{maxThr} + \epsilon}$
  - **Total** O_{total} global routing overflow values after routing (thresholds $O_{total\,Thr}$)
    - $P_{total} = \frac{O_{total} - O_{totalThr}}{O_{totalThr} + \epsilon}$
  - Combine with weight $w_{maxOverflow}$ and $w_{totalOverflow}$
    - $P_{overflow} = w_{maxOverflow} P_{max} + w_{totalOverflow} P_{total}$
- Hard constraints
  - Placement legality
    - Final placement must pass legality checks performed by checkPlacement: no cell overlaps, correct on-site placement and orientation, fixed I/O pins, and compliance with **soft placement blockages** and PDN constraints.
      - Within **soft blockage regions**, only physical/auxiliary cells (Filler cells, Well Tap Cells, Tie Cells and ENDCAP cells) and buffers/inverters are allowed to be placed.
  - Logical equivalence
    - The netlist must be logically equivalent; a logic equivalence check (LEC) will be performed.
  - No perturbation of the given floorplan is allowed
    - Blockages, PDN, Macro and I/Os must be the same as the input.
    - The component placement must be stitched into the provided floorplan .def (including PDN)

$$C_{HC} = \begin{cases} 1, \ if\ follow\ all\ hard\ constraints \\ 0, \ otherwise \end{cases}$$

- Final Score
  - $S_{final} = C_{HC} * (S_{PPA} - P_{ERC} - R - P_{dis} - P_{overflow})$

3.3.2 Scores

- All metrics except runtime use **pre_opt** (the input contest.def) as baseline; tool runtime and flow runtime use OpenROAD Flow (Figure 1 Left) as baseline.
- We exclude teams that directly use OpenROAD resizer **without any modifications** or the input contest.def as their solutions, and rank only teams that implement their own methods.

- For teams with illegal designs (i.e., failing equivalence or legality checks), the corresponding metric values are set to **1% worse than the worst value** among all teams and pre_opt for the same design.
    - Formally, Score_illegal = 1.01 * worst (Score_{pre_opt}, Score_{team})
- A design multiplier is applied (1.2 for ariane and 1.5 for bsg_chip) so that strong performance on more complex designs receives a higher score.
- **Results and scores of pre_opt and OpenROAD flow** on all testcases are shown here

Weights of each score component										
w_tns	w_dpower	w_lpower	w_slew	w_cap	w_fanout	w_flowRuntime	w_toolRuntime	w_maxOverflow	w_totalOverflow	w_dis
80	40	40	0.001	10	1	1	0.5	1	1	0.5

3.3.3 Platforms

- We will provide an evaluation environment for you via the Purdue Anvil supercomputer, with a specified number of CPU and GPU hours in your allocation, after successful Alpha submission. We expect participants to otherwise use their own resources for main development, and to use this provided resource for tuning and practice evaluation.
    - Purdue Anvil provides 128-core/128-thread AMD EPYC-7763 CPUs with NVIDIA A100 GPUs with CUDA 12.6 and Apptainer.
- The final evaluation environment will have stricter limits as defined below and will be run using the Apptainer environment:
    - 1 NVIDIA A100 GPUs (40 GB)
    - 16 physical CPU cores/threads
    - 64 GB memory
    - 200 GB disk
- Availability
    - Contestants **with university email addresses** can access these resources.
    - Teams that submit a working alpha can obtain resources, and those that submit a working beta can obtain more resources.
    - **Caveats:** (1) The planned resource availability is subject to change (e.g., with changes to U.S. government policy), and (2) the amount of resource per team may depend on the number of teams registering.
    - **We have provided a User Guide on how to use this resource for contestants with successful Alpha submissions.**
- The runtime limits will be determined after the alpha submission.

We will provide a Docker script that generates the Docker image, as well as a script to convert the Docker image to a Apptainer image. Along with that, we provide Docker and Apptainer images. We will use this Apptainer image for evaluation. **Contestants must build on top of this Docker or Apptainer environment.** For more details see the submission guideline.

4. Benchmarks

We will release a diverse set of 8 public benchmarks and 4 hidden benchmarks in the ASAP7 technology node with 7.5T multi-VT cell library. The benchmarks will vary in size from 15K - 1000K instances, including

- Macro-free designs **(4 public benchmarks)**
- Macro-containing designs **(4 public benchmarks + 4 hidden benchmarks)**

All public benchmarks are as follows

(Name, TCP, Util)	**Size**	**Macros (y,n)**	**PDN (y,n)**	**Blockages (y,n)**
AES, 250, 0.4	15K	N	Y	N
JPEG, 350, 0.7	50K	N	Y	N
AR37, 900, 0.3	0.1M	Y	Y	Y
AES_v2, 200, 0.4	15K	N	Y	**Y**
JPEG_v2, 450, 0.65	50K	N	Y	**Y**
AR37_v2, 950, 0.45	0.1M	Y	Y	**Y**
BSG_CHIP, 1200, 0.3	0.9M	Y	Y	**Y**
BSG_CHIP_v2, 1300, 0.5	1.4M	Y	Y	**Y**

5. Submission Guidelines

Environment setup. All participants must build on the Docker or Apptainer environment we provide. If additional packages are needed, include a **setup.sh** script that completes in under two hours to set up the environment. During the contest period, we will update the Docker/Apptainer environment with any major missing packages so participants do not need to install them.

Submission files. Each participant must submit a **ZIP file** containing setup.sh, run.sh and any additional data or code not already retrievable in setup.sh.

The ZIP file should be named **TeamID_solution.zip** and submitted via the Dropbox link. Contestants need to share the **cksum value** of the submission ZIP file via email (ispd26contest@gmail.com).

The run.sh must invoke your developed tool to read the input .lib, .lef, .v, .def and .sdc files and produce three outputs – modified .def, modified .v, and .changelist (see output formats) – in the directory specified by <output_dir>. The execution format should be:

run.sh <input_dir> <platform_dir> <output_dir> <top_module>

- *input_dir* contains the input design: contest.def, contest.sdc, and contest.v.
- *platform_dir* contains the ASAP7 enablement, in the same layout as Platform/ASAP7.
- *output_dir* is the empty directory in which you will place your <output_dir>/<design_name>.def and <output_dir>/<design_name>.v.
- *top_module* is the top module of the design.

6. Timeline

- Registration Open: Oct 1, 2025
- Release the first set of testcases, evaluation scripts and Dockerfile: Oct. 1, 2025
- Release the send set of testcases with blockages: Nov. 6, 2025
- Registration Close: Nov 30, 2025
- Release all public testcases: Dec. 3
- Alpha Submission Deadline: Jan 12, 2026 (Anywhere on earth)
- Beta Submission Deadline: Feb, 2, 2026 (Anywhere on earth)
- Final Submission Deadline: Mar, 7, 2026 (Anywhere on earth, and it is a hard deadline)
- Results Announcement: March 18, 2026

7. Contact

Email: ispd26contest@gmail.com

8. Registration

- ~~Please fill in this online registration form~~
- Registration window: Oct.1, 2025 - Nov 30, 2025

9. Contest Prizes

- First, second and third place winning teams will receive prizes consisting of cash and/or NVIDIA GPUs, with a total value of prizes at least USD $5000. Thanks to NVIDIA for their sponsorship of the ISPD26 contest prizes!

10. Organizers

- Andrew B. Kahng, Sayak Kundu, Yiting Liu, and Davit Markarian from UCSD
- Zhiang Wang from Fudan University
- Seonghyeon Park from POSTECH

11. Sponsors

- Purdue University and the NSF Chipshub: compute resources for teams and submission evaluation
- NVIDIA: prizes for winning teams

References

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